HARDWARE TECHNICAL REFERENCE

LS Pro

apricot

MITSUBISHI ELECTRIC

HARDWARE TECHNICAL REFERENCE

Published by
Apricot Computers Limited
3500 Parkside
Birmingham Business Park
Birmingham B37 7YS

MITSUBISHI ELECTRIC

Printed in the United Kingdom

Part no. 15050131

The Apricot LS Pro Technical Reference Manual is intended for:

Programmers and engineers involved in hardware and software design for LS Pro computers.

Service personnel involved in fault diagnosis and repair.

All computers in the Apricot LS Pro range are covered.

The manual is divided into a number of sections and appendices as described below:

1. Introduction This is a brief overview of the Apricot LS Pro which describes the options and major components of the system.

2. System Unit This section describes the system unit: it also includes disassembly instructions for servicing and replacing major components of the system. It includes pinouts of the connectors which appear on the rear of the system unit.

3. System Board This section provides an overview of the function of the system board and more detailed descriptions of the processor and interface circuitry. Sub-sections provide a description of each area of the board.

4. Peripheral Items This section describes each of the system components which attach to either the system board e.g. floppy disk drive, or system unit e.g. keyboard. Also included is brief information on the KeyLOC card. Sub-sections describe each component.

5. Memory and I/O space This section provides information on the usage of Memory and I/O space by the LS Pro system board, and programming information for each part of the system.

Appendices Three appendices are included:

Appendix A

This contains specifications for each component of Apricot LS Pro computers.

Appendix B

This appendix describes the differences between the revision C system board and the revision D system board described in section 3.

Appendix C

A list of error beep codes.

Preface

Associated Publications

The following publication may be of general use to engineers and programmers.

IBM Personal Computer AT Technical Reference Manual.

The following manufacturers data sheets give information on specific devices:

Intel	80386SX 80387SX 8042 Keyboard controller 82077 Floppy disk controller 8237 DMA controller 8254 System timers 8259 Interrupt controllers 82596 Ethernet coprocessor
VLSI	VL82C311 (SCAMP) AT chipset
Cyrix	486SLC
Cirrus	CL-GD542X video controller
National Semiconductor	NS16450 Serial communications controller
Hitachi	MC146818 Real time clock

CONTENTS

Contents

Contents

General

The Apricot LS Pro family is a range of ultra-compact IBM compatible computers which can be used as a personal computer, a network workstation or a high resolution graphics workstation.

The main features of the system are:

- 80386SX or 486SLC microprocessor operating at up to 33MHz.
- 2 to 16 Mbytes of on-board RAM.
- IBM compatible serial port.
- IBM compatible parallel port.
- Ethernet port.
- Token-Ring port (optional).
- PS/2 compatible mouse port.
- Floppy disk controller on system board.
- Hard disk connector on system board.
- Full IBM functional compatibility.
- On-board VGA.
- On-board high resolution video.
- Internal power supply.
- LOC Technology security sub-system.
- Socket for 80387SX.
- Windows 3.1 compatible Business Audio subsystem.

Variants

The basic system unit may be fitted with:

- 2 to 16 Mbytes of RAM.
- 80, 120, 170, 240 or 540 Mbyte hard disk drive.
- 3.5 inch floppy disk drive.
- 80387SX coprocessor.

A VGA monitor will be required. To take advantage of the high resolution video modes a suitable SVGA or EVGA monitor will be required.

System unit

The system unit contains: the processor(s), the system memory, disk drives, power supply, security circuitry and interfaces to keyboard, monitor and peripherals. All the interface circuitry except the Token-Ring network interface is on the system board.

Dedicated connectors are provided on the system board for a Token-Ring module.

A block diagram of the system unit is shown at the end of this section. It shows the components of the system and identifies functions implemented on the system board.

Keyboard

The keyboard is a full QWERTY typewriter keyboard and numeric keypad together with editing keys. The layout of the 102 key UK keyboard is compatible with the IBM AT enhanced keyboard.

The keyboard is fitted with a PS/2 style miniature DIN connector and any fully compatible keyboard can be plugged into the system unit.

Monitors

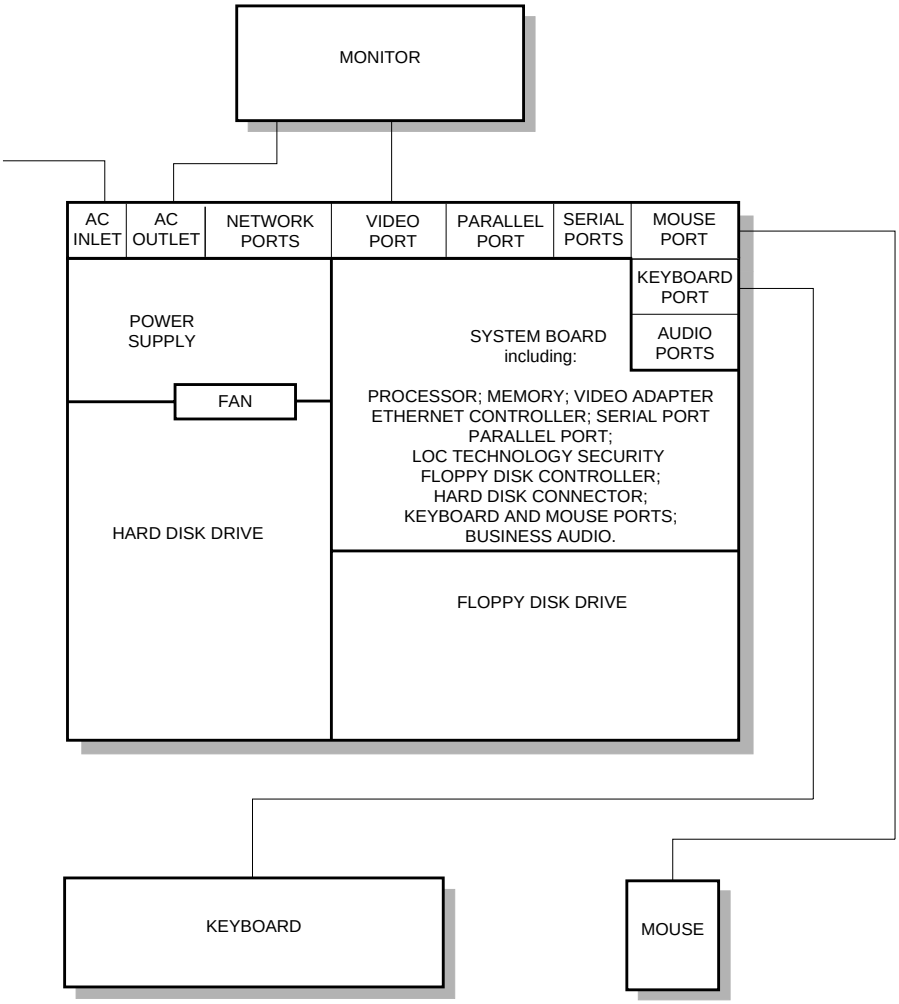
The system board is fitted, with a VGA video interface which will drive any suitable monochrome or colour analogue monitor.

The on-board VGA controller also supports high resolution video modes. To take advantage of the higher resolution video modes an SVGA or EVGA monitor must be used. Video drivers for popular software packages are available.

Expansion

System RAM may be expanded to 16 Mbytes by fitting SIMMs.

A socket for an 80387SX coprocessor is fitted on the system board.



Contents

2 SYSTEM UNIT

Introduction

The main components of the system unit are:

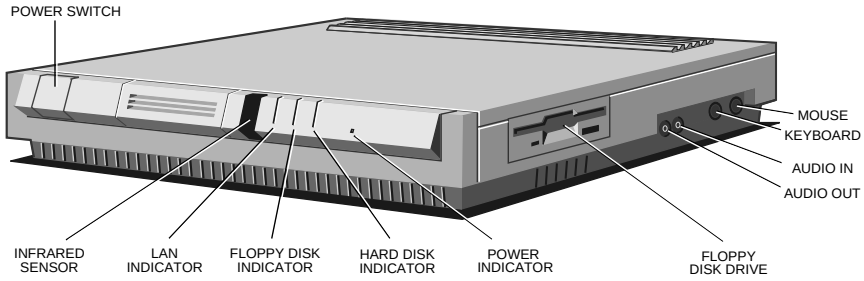
- base
- top cover
- system board
- disk drives
- power supply

The top cover is easily removed without any tools.

The system board contains all the processing and interface circuitry and the system RAM. 2 or 4 Mbytes of RAM is soldered to the board and SIMMs can be fitted to increase the total amount of system RAM to a maximum of 16 Mbytes.

External layout

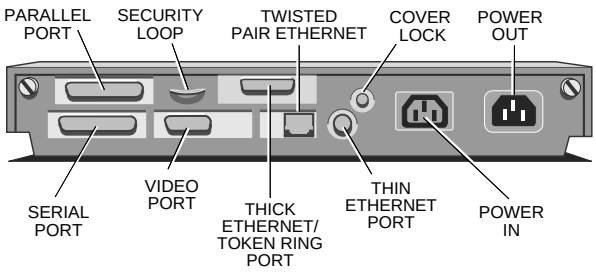
The front panel of the system unit contains: the power switch and slots for four LEDs and the IR detector for the security card. The right side panel contains the keyboard and mouse ports, and the audio input and output sockets.



The floppy drive bezel is on the right side of the system unit.

The rear panel contains the following connectors: mains power input; auxiliary power outlet; monitor; Ethernet ports; serial port; parallel port.

The layout of the rear panel is shown in the illustration below.

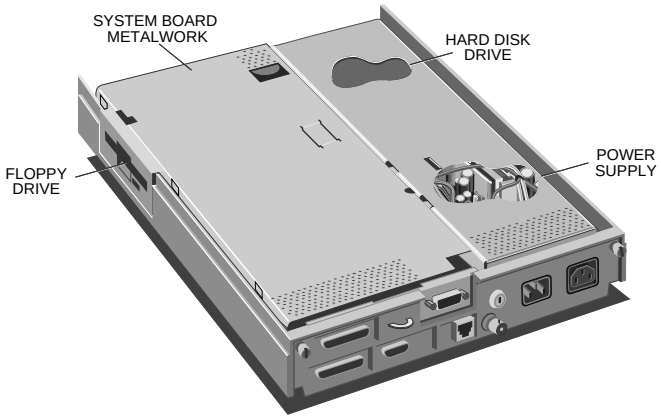


Illustrations and pinouts of the connectors on the rear panel are given at the rear of this section.

Internal layout

The layout of the inside of the system unit is shown in the illustration below. At the front left of the system unit is the hard disk drive. Behind the hard disk drive is the power supply unit. Both the power supply and the hard disk drive are beneath a metal cover.

The floppy drive is at the front right of the system unit attached to a metal plate which extends the full length of the system board.



Servicing level

The level of information in this section is intended to enable suitably qualified personnel to remove and replace major components of the system unit and to access components to install add-ons.

Dismantling and re-assembly

The LS Pro range has been designed to meet international EMI and safety standards.

Warnings and cautions

To ensure safety and continued compliance with these standards, observe the following precautions.

- It is recommended that modifications are carried out by an authorized dealer. Unqualified users should not normally dismantle the equipment.
- Replacement parts should be of the type and rating specified by the manufacturer.
- All earth connections must be maintained to the original specification.
- Ensure that all personnel concerned are familiar with the action to be taken in the event of electric shock.

Warning

Never carry out any work on the equipment with power applied. Always switch off at the mains and remove the power lead from the equipment before starting work.

Note

Any reference to left or right during dismantling and re-assembly assumes that the reader is viewing the unit from the front, unless otherwise stated.

Antistatic precautions

All electronic components and equipments are sensitive to static electricity. Even small electrostatic discharges can render components useless or severely shorten their working life, therefore preventive measures should always be taken.

No work should be carried on any item unless it is in a Special Handling Area (SHA) as defined in BS CECC 00015:Part 1. In general this involves:

- a common earth point
- an earthed bench or bench mat
- an earthed wrist strap

Equipment required

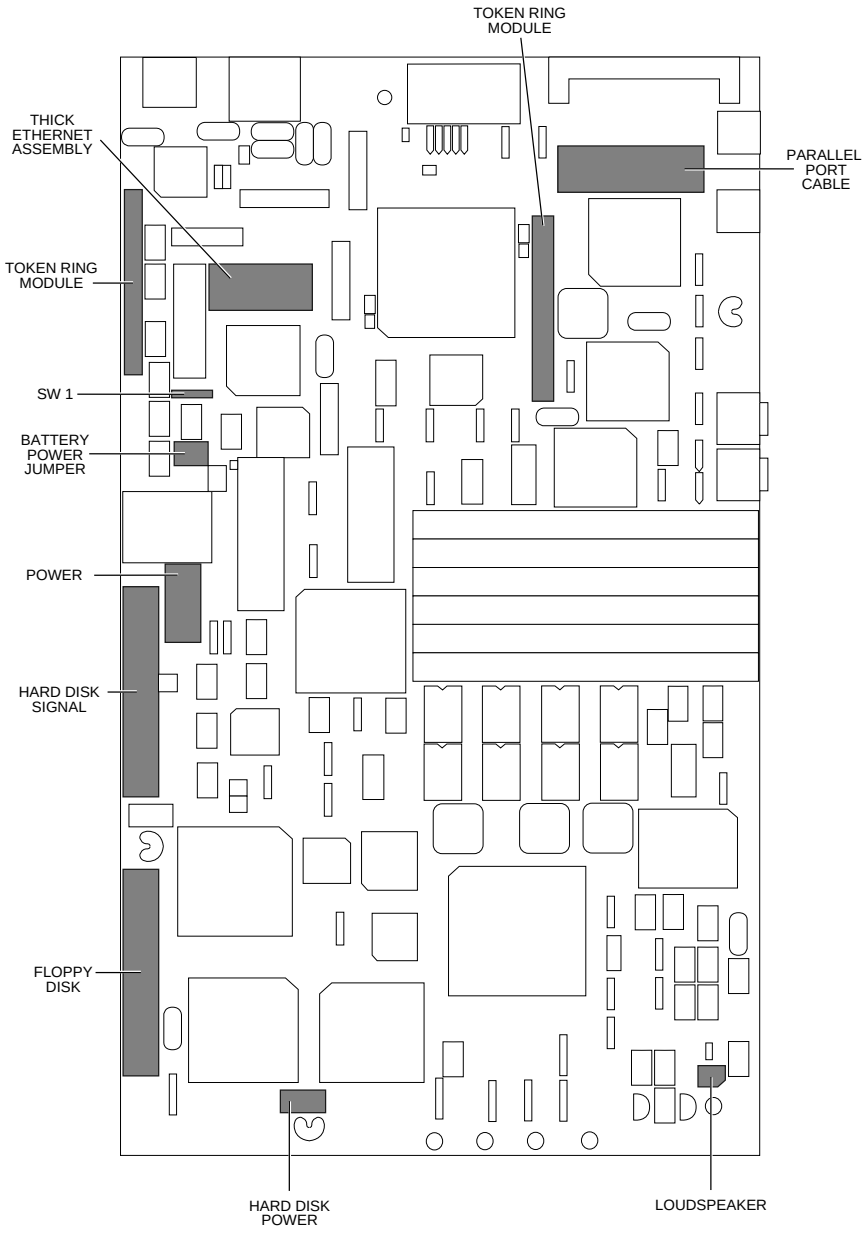
The following tools are required to dismantle the system unit.

- Philips screwdriver
- Flat-bladed screwdriver
- Nut spanner set
- thin nosed pliers

System board connectors

Many of the dismantling/reassembly procedures which follow involve the disconnection and reconnection of system board plugs and sockets. The following table gives, for each socket, the connector number which identifies it. This number is printed on the system board next to each connector.

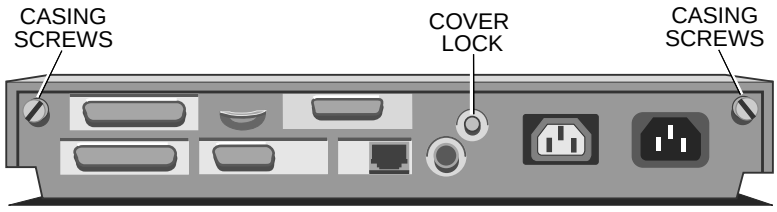
Connector	Label
Parallel port	PL8
Token ring module	PL9 and PL16
Hard disk drive power	PL12
Thick Ethernet	PL13
System board power	PL15
Hard disk drive control	PL17
Floppy disk drive	PL18
Loudspeaker	PL40



Removing the system unit top cover

A keylock on the rear panel of the system unit locks the top cover in place. The cover cannot be removed unless this is unlocked. The cover is located by a ledge at the front and lugs on the sides and at the rear. Two thumbscrews in the rear panel secure the cover.

The following illustration shows the thumbscrews and keylock.



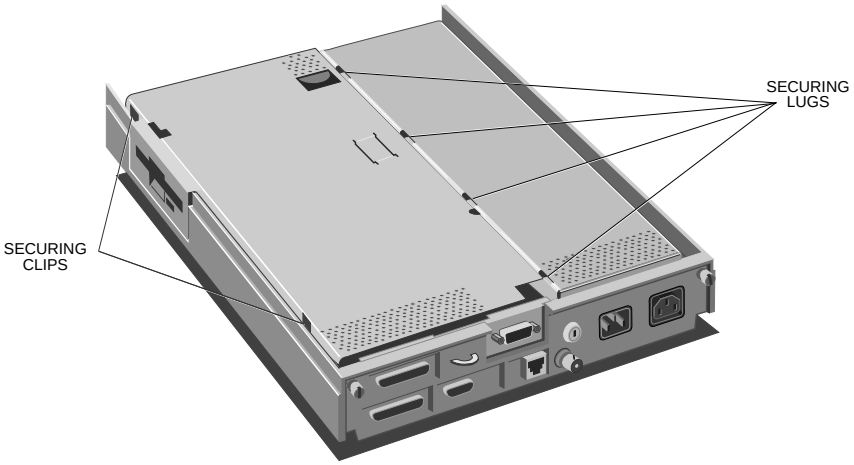
1. Check that the system unit power switch and mains supply are switched off and disconnect the mains supply.
2. Ensure that the keylock on the rear panel is unlocked.
3. Loosen the two thumbscrews at the top of the rear panel. If they have been done up tightly it may be necessary to use a screwdriver to loosen them.
4. Slide the top cover forward a few millimetres and lift it clear.
5. Replacing the top cover is simply the reverse of removal. Check that the keylock is in the unlocked position. Make sure that the top cover is properly aligned during replacement and do not force it into position.

Note

It is not necessary to remove cables (other than the mains power cable) to remove the system unit top cover. However, in order to remove some of the internal components external cabling must be removed.

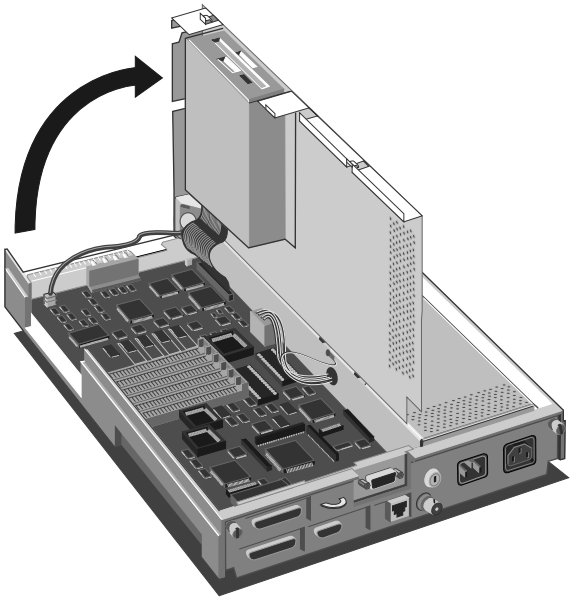
Removing the system board metalwork

The system board metalwork is secured to the power supply metalwork by lugs, and by clips to the system unit base.



1. Remove the system unit top cover.
2. Release the two retaining latches. On releasing the latches, the system board metalwork will spring up slightly.

3. Hinge the system board metalwork to the vertical as shown below:

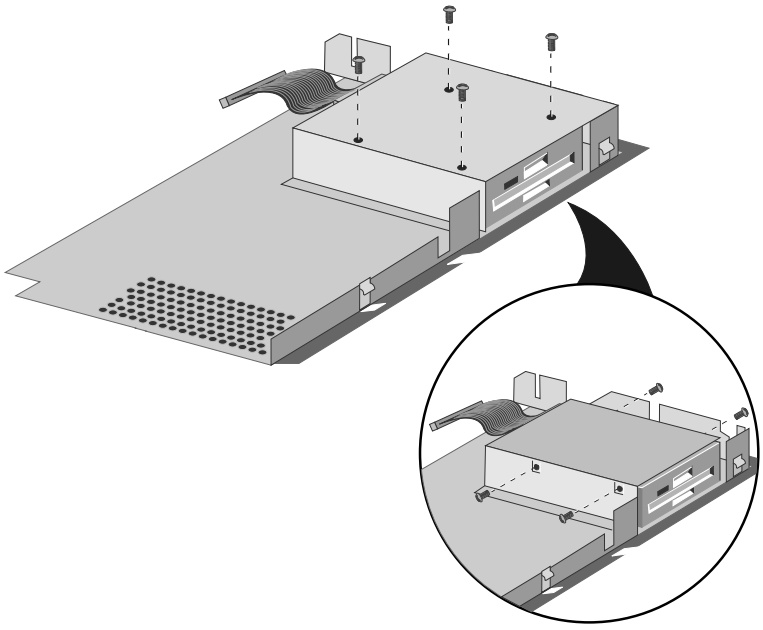


4. Disconnect the loudspeaker cable from the system board.
5. If your system is fitted with a floppy disk drive disconnect the ribbon cable at the system board taking care not to strain the cable or its connectors.
6. Lift the system board metalwork clear of the computer.
7. Invert the system board metalwork, and rest it on a flat surface.
8. Replacement is simply the reverse of removal. Take care to ensure that the metalwork engages correctly. Do not use undue force. Route the loudspeaker cable between the front of the system unit and the LEDs.

Removing the floppy drive

The floppy drive is mounted in the metalwork above the system board.

Two variants of metalwork have been used, they are both shown in the illustration below.

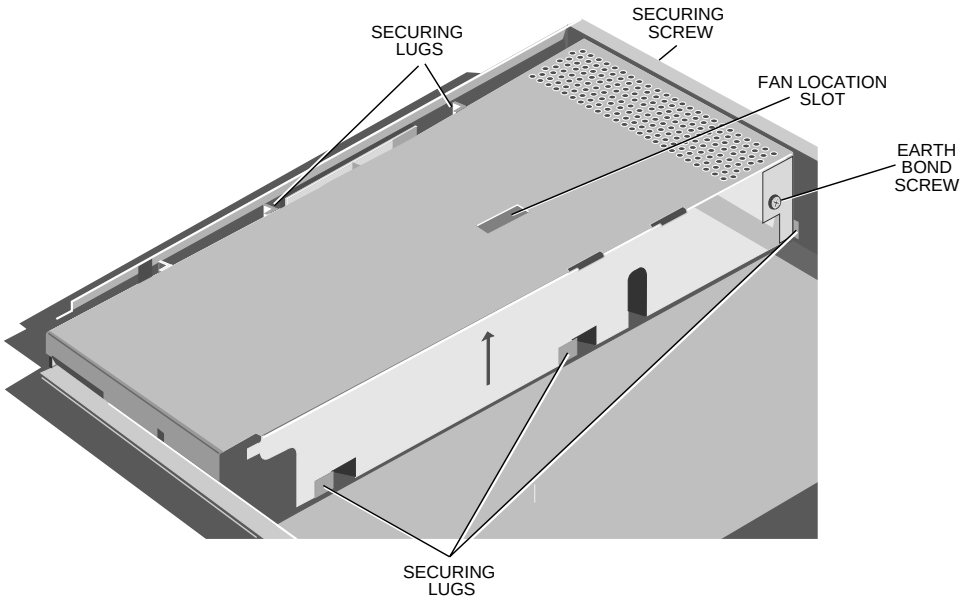


1. Remove the system board metalwork.
2. Remove the four screws which secure the floppy drive and remove the drive.
3. Replacing the floppy drive is simply the reversal of removal. If the drive being installed is a replacement ensure that the drive select switch on the side of the drive is in the same position as that on the old drive.

Removing the power supply metalwork

The power supply metalwork covers the top of the power supply and divides the system unit, it applies gentle pressure to the top of the system unit fan. The system board metalwork uses the power supply metalwork for location.

The power supply metalwork is secured by two screws and a number of lugs.



1. Remove the system board metalwork.
2. Remove the earth bond screw which secures the system board escutcheon plate to the power supply metalwork.
3. Remove the screw in the rear panel between the mains inlet and outlet which secures the power supply metalwork.
4. Slide the power supply metalwork forward by approximately 6mm to free the lugs.
5. An earth cable connects the power supply to the metalwork. Gently lift the metalwork and carefully turn it over.
6. Remove the screw which secures the cable to the metalwork and lift the metalwork clear.

7. Replacement is the reverse of removal. However care must be taken to note the following:

> **Warning**
>
> *Remember to reconnect the power supply earth cable to the metalwork.*

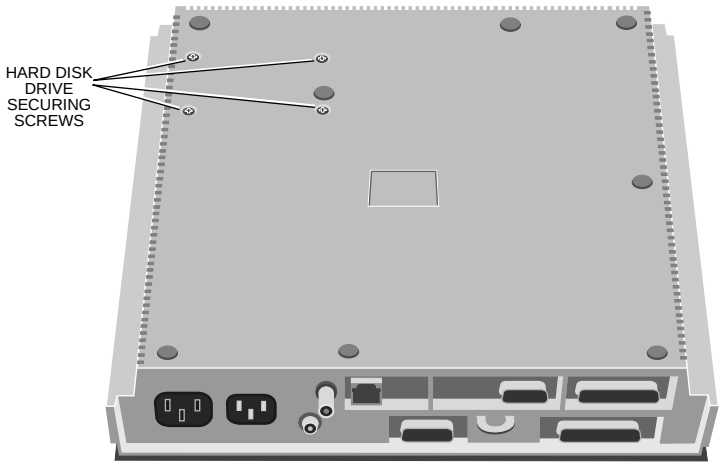
- The metalwork must be behind the switch operating lever of the power switch linkage.
- A metal RFI screening tray is fitted in the base of the system unit. During the replacement of the power supply metalwork the front edge of the tray can be damaged.

  In order to prevent damage occurring use a piece of card to hold down the fingers at the front edge of the metalwork while the metalwork is replaced. Once the metalwork is in place gently remove the card.
- Take care to ensure that the lugs on the bottom right of the metalwork are properly engaged and that the metalwork does not foul on the fan.

  The fan rests on a flexible foam pad which is compressed when the power supply metalwork is in place. A slot is provided in the metalwork to allow a small blunt instrument (flat bladed screwdriver) to push the fan down during the replacement of the metalwork. Do not force the power supply metalwork into position.

Removing the hard disk drive

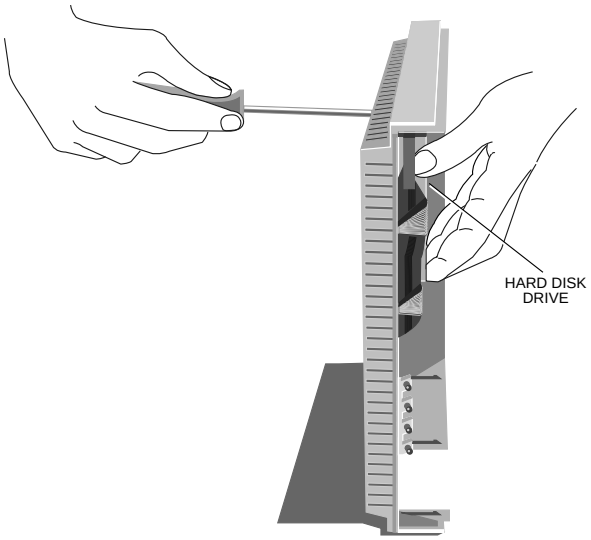
The hard disk drive is attached to the system unit base by four screws on the underside of the system unit. The following illustration identifies the screws which hold the hard disk drive in place.



1. Remove the system unit top cover, system board metalwork and power supply metalwork.
2. Disconnect the hard disk drive power and signal cables from the system board.

> **Warning**
>
> *Do not attempt to disconnect the cables from the drive with the drive still in the system unit. Attempting to do so will damage the drive circuit board.*

3. Holding the hard disk drive firmly in position carefully turn the system unit onto one side and remove the four screws which secure it.



4. Still holding the disk drive, carefully turn the system unit back and rest it on the work surface.
5. Slide the hard disk drive to the right to clear the power supply metalwork and lift the hard disk drive out of the system unit complete with the power and signal cables.
6. Replacing the hard disk drive is simply the reverse of removal. If the drive being installed is a replacement ensure that the drive select jumpers are in the same positions as those on the old drive.

Warning

1. *Reconnect the power and signal cables to the drive before putting the drive in position.*
2. *Ensure that the screws which you use to secure the drive are the ones which you removed. If you use longer screws you will damage the drive.*

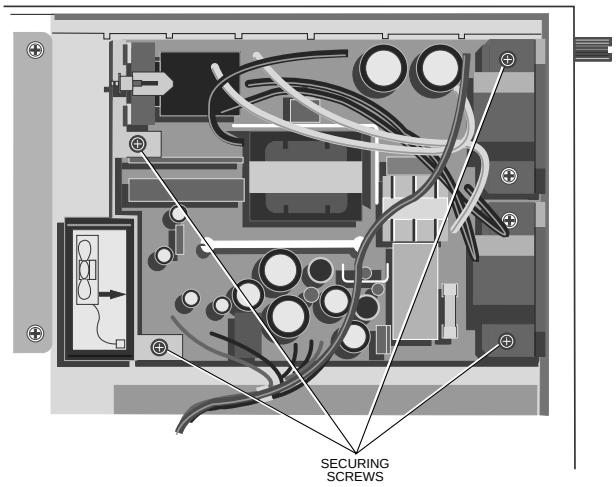
Removing the fan

The cooling fan rests on a flexible foam pad and is located in the base of the system unit by small ribs. Gentle pressure from the power supply metalwork ensures that the fan is held in place.

1. Remove the power supply metalwork.
2. Disconnect the fan power connector from the PSU.
3. Remove the fan.
4. Replacement is simply the reverse of removal. Make sure that you replace the fan in the same orientation as it was before removal, and that the fan power cable is secured to the fan with a cable tie.

Removing the power supply

The power supply is secured to the bottom of the system unit by four screws. The following illustration identifies the screws that must be removed and the connectors that must be disconnected in order to remove the power supply.

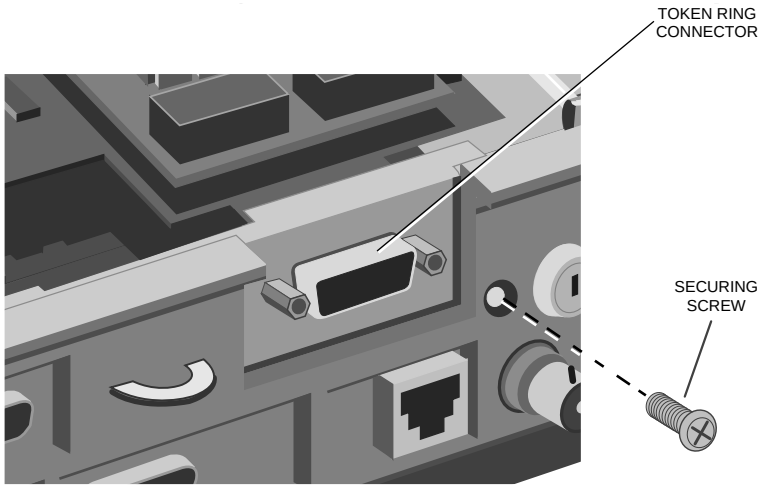


1. Remove the power supply metalwork.
2. Disconnect the system board and fan power connectors.
3. Lift out the fan.
4. Remove the four screws securing the power supply.
5. Lift the power supply clear of the system unit.
6. Replacement is simply the reverse of removal. Ensure that the voltage range selection jumper is in the correct position for the mains supply available. The jumper is identified in section 4 of this manual.

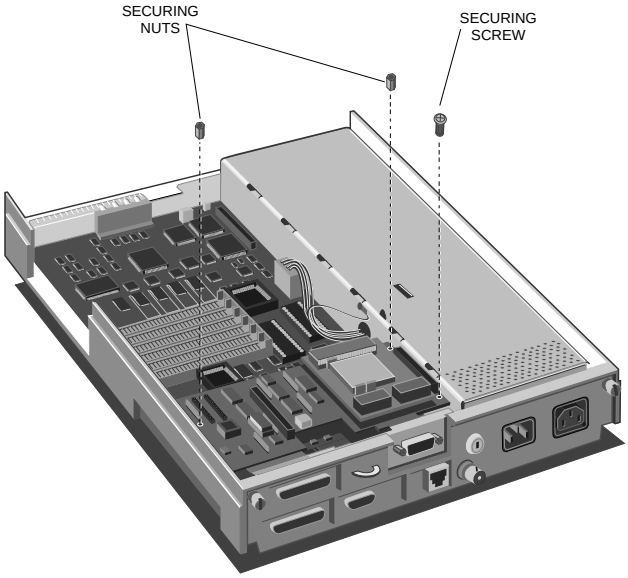
Removing a Token-Ring module

The Token-Ring module is secured to three standoff pillars inside the system unit, and to the escutcheon plate at the rear of the system unit. To remove the module follow the instructions below:

1. Remove the system board metalwork.
2. Remove the screw in the rear panel of the system unit, to the right of the Token-Ring connector.



3. Remove the screws and nuts which secure the module to the standoff pillars.



4. Gently remove the module.

Note

Care must be taken to ensure that the module is removed vertically. Any horizontal movement will damage the connectors.

Read the following paragraphs before replacing the module.

The Token-Ring module connectors have three components: the connectors on the system board, the connectors on the Token-Ring module, and the pin assemblies which connect them. When you remove the Token-Ring module the pin assemblies will probably come out with the Token-Ring module, although they may remain in the system board.

When the Token-Ring module is in position the plate that surrounds the Token-Ring connector is between the system unit base and the escutcheon plate. The two standoff pillars by the connector nearest the power supply, protrude through corresponding holes in the Token-Ring module.

It is vital that during replacement the Token-Ring module is correctly aligned. Any misalignment will damage the connectors and/or the module. When replacing the module make sure that the plate is inserted correctly and that the standoff pillars are correctly aligned. Check that the connectors are correctly aligned, then gently insert the module.

Warning

Take care not to exert undue pressure when inserting the module.

Removing a parallel port cable

The parallel port cable is secured to the escutcheon plate by the two D-type connector screwlocks. To remove the cable:

1. Remove the system board metalwork.
2. Remove the two screwlocks in the parallel port connector.
3. Unplug the cable from the socket on the system board and lift the cable clear.
4. Replacement is simply the reverse of removal.

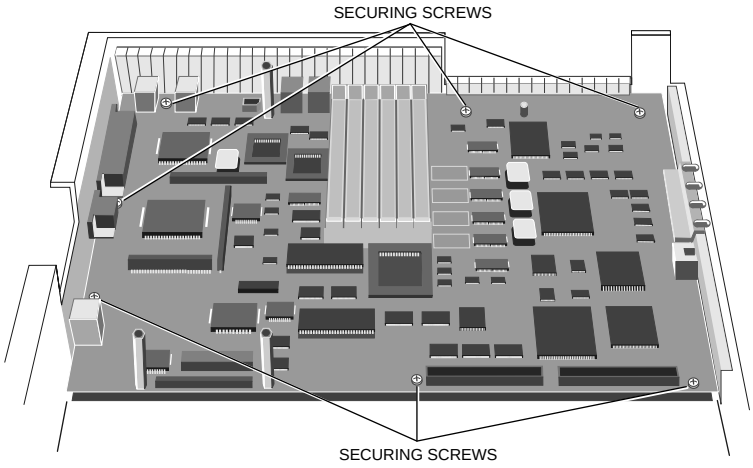
Removing a thick wire Ethernet assembly

The thick wire Ethernet assembly is secured to the escutcheon plate at the rear of the system unit. To remove the assembly follow the instructions below:

1. Remove the system board metalwork.
2. Remove the screw that secures the thick wire Ethernet assembly to the escutcheon plate, unplug the assembly cable from the system board, and lift the assembly clear of the system unit.
3. Replacement is simply the reverse of removal.

Removing the system board

The system board is secured to the base of the system unit by seven screws through the system board and four screwlocks through the escutcheon plate. The following illustration identifies the positions of the system board screws.



1. Remove the system unit top cover and put the system cover lock in the locked position.
2. Remove the system board metalwork and disconnect all system board connectors.
3. Remove the parallel port cable and thick cable Ethernet assembly or Token-Ring module (if fitted).
4. Remove the seven screws which secure the system board.
5. Remove the screwlocks that secure the video and serial port connectors.
6. Remove the lock nut on the thin Ethernet connector.
7. Carefully lift the system board clear of the system unit.

Notes

1. *If the system cover lock is not in the locked position the system board will foul during removal.*
2. *During removal the audio connector may foul on the RFI isolation tray. If so, press the isolation tray against the side of the system unit base to allow the connectors clearance.*

7. Replacement is simply the reverse of removal.

Ensure that all the switches and jumpers on a replacement board are in the correct position.

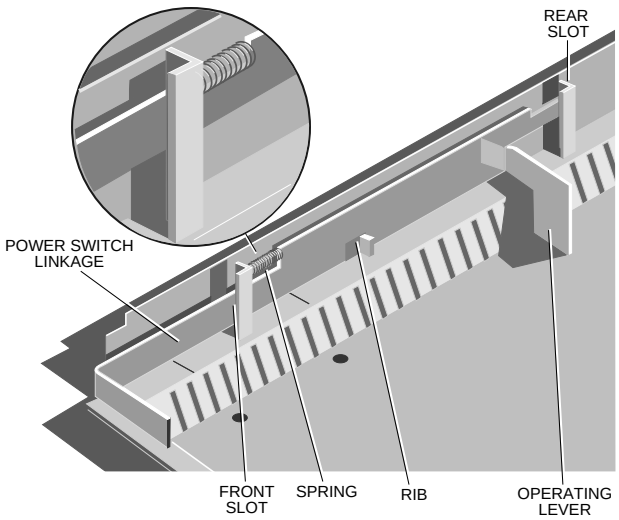
Removing an escutcheon plate

The escutcheon plate at the rear of the system unit is secured by three screws to the rear of the system unit base. To remove the escutcheon plate:

1. Remove the system board metalwork.
2. Remove the system board.
3. Remove the screw that secures the escutcheon plate to the power supply metalwork.
4. Remove the three screws that secure the escutcheon plate to the system unit, and lift the escutcheon plate clear.
5. Replacement is simply the reverse of removal.

Removing the power switch linkage

The power switch linkage mechanically links the system ON/OFF switch on the front of the system unit to the power supply ON/OFF switch. It is located in two slots in the system unit base plastics. The linkage must clear a rib on the side of the base plastics during removal, and another during replacement. To remove the linkage:

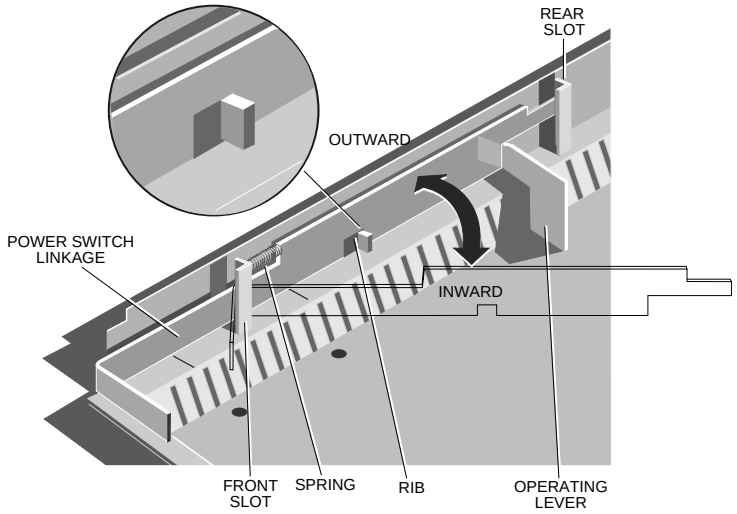


1. Remove the system unit top cover, system board metalwork, hard disk drive, power supply metalwork, fan, power supply and system board.

Warning

During the following instructions do not apply excessive pressure or the linkage may be deformed or the plastics break.

2. Using a pair of thin nosed pliers, disconnect the spring and put it somewhere safe.
3. Exerting gentle inward pressure on the operating lever, slide the power switch linkage forward past the rear of the two ribs, far enough to free the back of the linkage from the rear slot.
4. Slide the linkage back bending it gently to allow it to pass to the right of the rear slot and push it as far back as it will travel.



5. With the 90° bend at the front of the linkage against the front of the two slots swing the rear of the linkage into the centre of the system unit.

   Note

   There should be no resistance to this movement. If there is resistance you have not pushed the linkage far enough back.

6. Slide the linkage back through the slot and lift it clear.
7. Replacement is simply the reverse of removal except that gentle inward pressure must be exerted to the front of the linkage to allow it to pass the front rib. Do not force the linkage into place.

RFI screening tray and insulation sheet

The LS Pro system unit base is fitted with a metal RFI screening tray and a plastic insulation sheet during manufacture. The metal tray reduces RFI emissions from the system unit and ensures compliance with international regulations.

The plastic sheet insulates components inside the system unit from the RFI tray. Both components are essential.

There should never be any need to remove the tray or the screening sheet. However if you do need to remove them you must ensure that they are replaced correctly when you reassemble the system.

Insulation sheet

The plastic insulation sheet rests on the isolation tray and is not secured until the other system unit components are installed. Correct positioning of the sheet can be ensured by checking that the screw holes in the sheet align with those in the RFI tray, and the system unit base.

RFI screening tray

The RFI screening tray sits in the system unit base, it is only secured by double sided tape at the front left of the system unit, in front of the hard disk drive.

Since the tray includes cut-outs for all the system unit connectors, the correct orientation should be obvious. Ensure that the connector cut-outs and the screwholes in the base of the tray are all correctly aligned with the system unit base. Then secure the front left edge of the tray with the double-sided tape.

Installing add-ons

Memory upgrades

During manufacture 2 or 4 Mbytes of RAM can be soldered to the system board. System board memory can be expanded to a maximum capacity of 16 Mbytes by fitting SIMMs in sockets provided on the system board.

When 4 Mbytes of RAM is installed during manufacture four SIMM sockets are fitted. When 2 Mbytes of RAM is installed six SIMM sockets are fitted.

SIMMs must be installed in pairs, upgrades of 2 and 8 Mbytes are available. The 2 Mbyte upgrade contains two 60nS 1Mx9 SIMMs, the 8 Mbyte upgrade contains two 60nS 4Mx9 SIMMs.

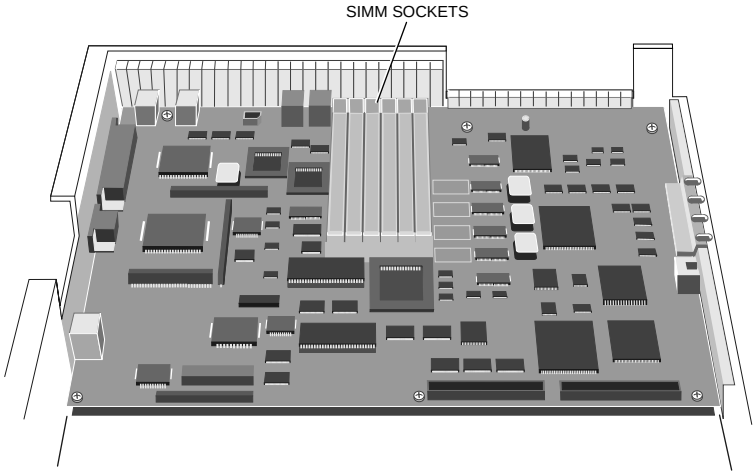
The following table identifies the valid upgrade combinations.

System board capacity (Mbytes)	Upgrade to (Mbytes)	Bank			Note
		1	2	3	
2	4	2	-	-	
2	6	2	2	-	
2	8	2	2	2	1
2	12	2	8	-	
2	16	-	8	8	2
4	6	N/A	2	-	
4	8	N/A	2	2	1
4	12	N/A	8	-	
4	16	N/A	8	8	2

Notes

1. *For both system board RAM capacities an alternative method of achieving 8 Mbytes of RAM is to install an 8 Mbyte upgrade in bank 2 and leave the other bank (or banks) empty. This configuration disables the RAM soldered to the system board.*
2. *When banks 2 and 3 are both occupied by 8 Mbyte upgrades the RAM soldered to the system board is disabled.*

The SIMM connectors are located on the right side of the system board just behind the floppy drive bezel as shown in the following illustration.



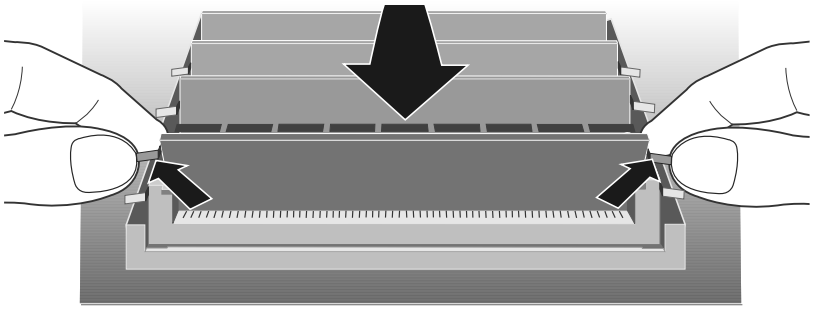
Note

When removing and installing SIMMs it is easiest to work with the rear of the system unit towards you. As a result the following instructions assume that you are viewing the system unit from the rear.

Removing SIMMs

If you wish to install an upgrade in a pair of SIMM sockets which are already occupied you must first remove the existing SIMMs. Starting with the SIMM nearest the rear of the system unit and working towards the front:

1. Lever the metal clips on each side of the socket gently away from the SIMM using your thumbnails. When the clips are far enough apart the top edge of the SIMM will move backwards until the SIMM is at an angle of about 15°.



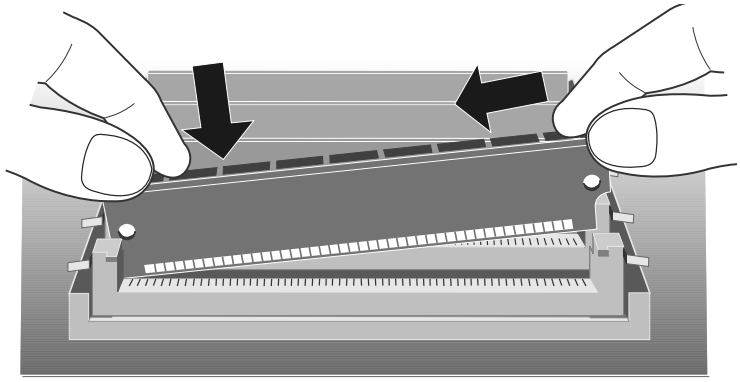
2. Taking care to avoid touching any of the components on the SIMM grip the top corners of the SIMM between thumb and first finger and carefully pull the SIMM out of the socket.
3. Repeat steps 1 and 2 for the other SIMM(s) affected.

Inserting SIMMs

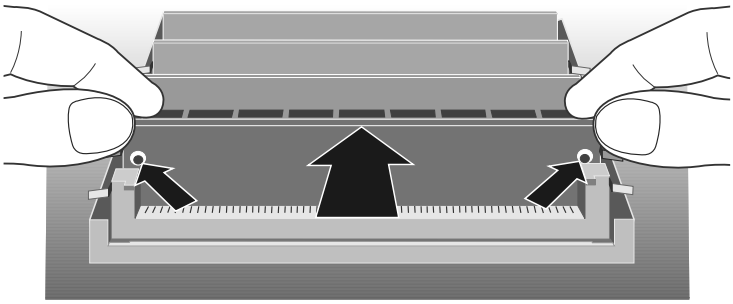
From the illustrations showing the possible SIMM combinations decide which SIMM capacity will be installed in each bank. Then, working from the socket nearest the front of the system unit towards the rear, install the SIMMs.

To fit a SIMM:

1. Hold the SIMM so that the memory chips are facing the front of the system unit with the metal connector strip nearest the system board.
2. Position the SIMM above the socket at an angle of about 15°.



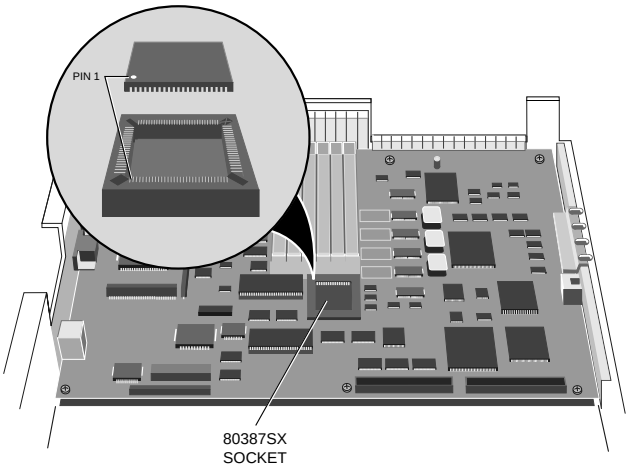
3. Lower the SIMM towards the socket. The right edge of the SIMM will be prevented from reaching the connector by the securing clip.
4. Allow the left edge of the SIMM to drop into the connector.
5. Push the SIMM gently to the right and lower the right edge into the connector.
6. Ensure that the SIMM is properly located in the connector.
7. Rotate the SIMM into the vertical position by pushing gently on the top corners.



8. If the SIMM is properly located the SIMM should remain in position held by the securing clips, and with a small plastic lug through the holes on either side of the SIMM.

Installing an 80387SX

1. Remove the system unit top cover.
2. Remove the system board metalwork.
3. Locate the 80387SX socket from the following illustration.



4. The 80387SX has a positioning guide in the form of a circular recess. Insert the 80387SX in the socket with the positioning guide at pin 1 making sure that you do not bend or otherwise damage the pins.

   Note

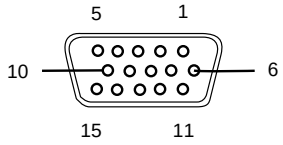
   The 80387SX only fits in one orientation. Do not use excessive force or damage may occur.

5. Reassemble the system.

System unit connectors

The following illustrations and tables show the layout, pin numbering and pinout of each of the connectors on the rear panel of the system unit.

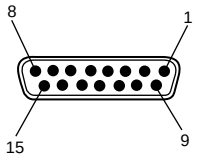
VGA The VGA display connector is a 15-pin D-shell.



Pin	I/O	Output	Mono	Colour
1	O	Red	No pin	Red
2	O	Green	Mono	Green
3	O	Blue	No pin	Blue
4	NA	Reserved	No pin	No pin
5	NA	Digital Gnd	Self Test	Self Test
6	NA	Red rtn	Key pin	Red rtn
7	NA	Green rtn	Mono rtn	Green rtn
8	NA	Blue rtn	No pin	Blue rtn
9	NA	Plug	No pin	No pin
10	NA	Digital Gnd	Digital Gnd	Digital Gnd
11	NA	Reserved	No pin	Digital Gnd
12	NA	Reserved	Digital Gnd	No pin
13	O	Hsync	Hsync	Hsync
14	O	Vsync	Vsync	Vsync
15	NA	Reserved	No pin	No pin

Ethernet *Thick*

The thick Ethernet connector is a 15-pin female D-shell which uses a slide to hold the male and female connectors together.



Pin	I/O	Signal
1	NA	Collision presence shield
2	I	Collision presence (+ve)
3	O	Transmit (+ve)
4	NA	Receive shield
5	I	Receive (+ve)
6	NA	Power return
7	NA	Reserved (+ve)
8	NA	Reserved shield
9	I	Collision presence (-ve)
10	O	Transmit (-ve)
11	NA	Transmit shield
12	I	Receive (-ve)
13	NA	Power
14	NA	Power shield
15	NA	Reserved (-ve)

Thin

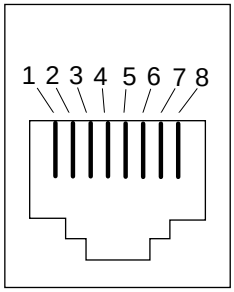
The thin Ethernet connector is a BNC socket.

Core	Signal
Shield	Return

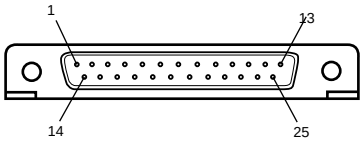
Twisted pair (TPE)

The unshielded twisted-pair Ethernet port is an RJ45 connector.

Pin	Function
1	Transmit data +
2	Transmit data -
3	Receive data +
4	Not used
5	Not used
6	Receive data -
7	Not used
8	Not used



Serial The serial port uses a male 25-pin D-shell connector.



Pin	I/O	Signal name
2	O	Transmit data (COM1)
3	I	Receive data (COM1)
4	O	Request to send (COM1)
5	I	Clear to send (COM1)
6	I	Data set ready (COM1)
7	NA	Signal ground
8	I	Data carrier detect (COM1)
12	I	Data carrier detect (COM2)
13	I	Clear to send (COM2)
14	O	Transmit data (COM2)
16	I	Receive data (COM2)
19	O	Request to send (COM2)
20	O	Data terminal ready (COM1)
22	I	Ring indicate(COM1)

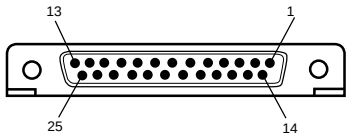
All other pins are not connected.

Note

The Rev C system board does not provide the COM2 signals.

Parallel port

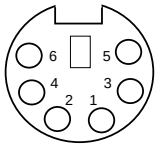
The parallel port uses a female 25-pin D-shell connector.



Pin	I/O	Signal name	Pin	I/O	Signal name
1	I/O	Strobe	14	O	Autofeed XT-
2	I/O	Data bit 0	15	I	Error-
3	I/O	Data bit 1	16	O	Init-
4	I/O	Data bit 2	17	O	Slct In-
5	I/O	Data bit 3	18	NA	Ground
6	I/O	Data bit 4	19	NA	Ground
7	I/O	Data bit 5	20	NA	Ground
8	I/O	Data bit 6	21	NA	Ground
9	I/O	Data bit 7	22	NA	Ground
10	I	Ack-	23	NA	Ground
11	I	Busy	24	NA	Ground
12	I	PE	25	NA	Ground
13	I	SLCT			

Keyboard/mouse connectors

The keyboard and mouse connectors are miniature 6-pin DIN connectors.



Pin	I/O	Signal name
1	I/O	Data
2	NA	Reserved
3	NA	Ground
4	NA	+5Vdc
5	I/O	Clock
6	NA	Reserved

Contents

3.1 INTRODUCTION

General

This section describes the LS Pro system board and the operation of its processing system and interface circuits.

The LS Pro range uses a highly integrated, IBM AT compatible system board. In addition to standard features, the LS Pro system board provides: Ethernet interface, business audio subsystem, LOC Technology security subsystem and a mouse port.

System Identification Number (SIN)

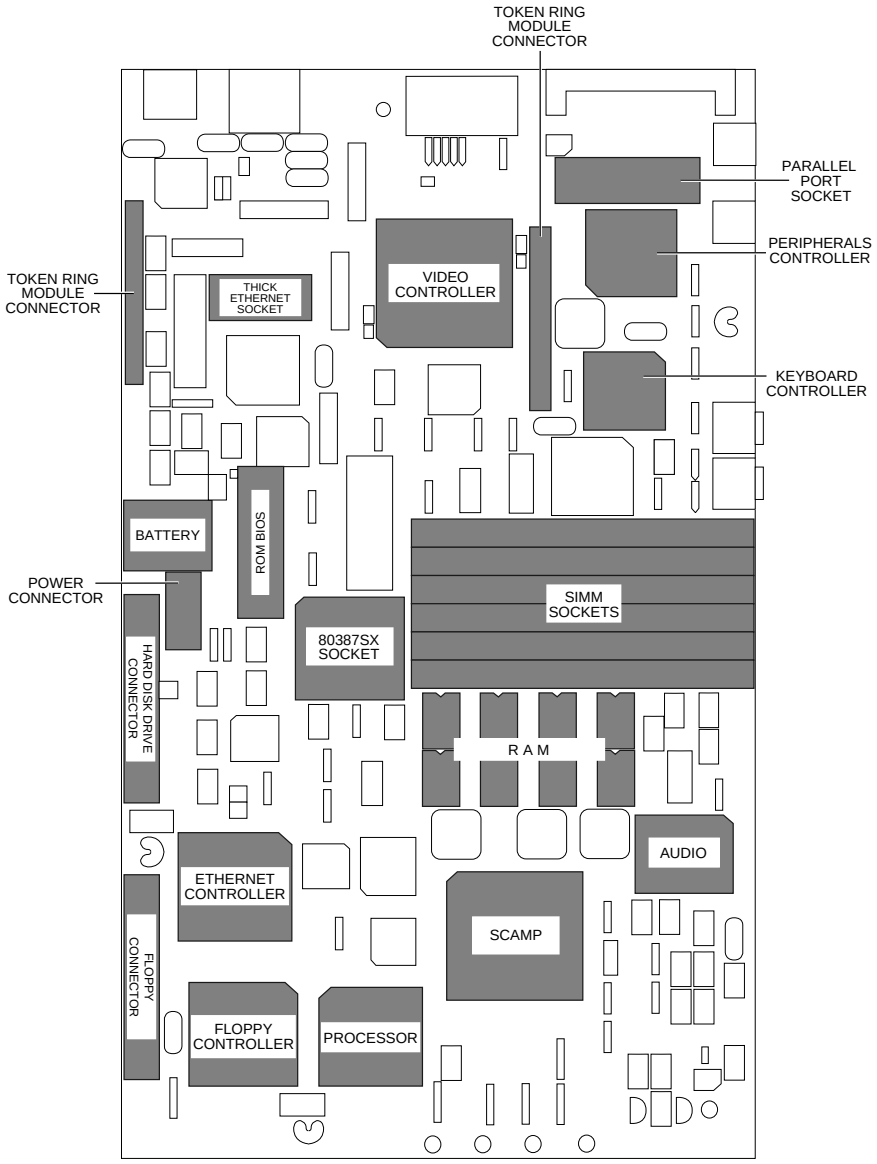
Each system board fitted with the LOC Technology subsystem is identified by its own System Identification Number (SIN). During normal operation the SIN will never be required. Under certain circumstances the system may display a prompt asking for the SIN to be entered. If this happens refer to the Owner's Handbook and associated documentation. If Apricot's LOC Technology software is in use refer to the documentation supplied with the software.

Major components

The following list of major components on the system board identifies the custom chips and briefly details their function:

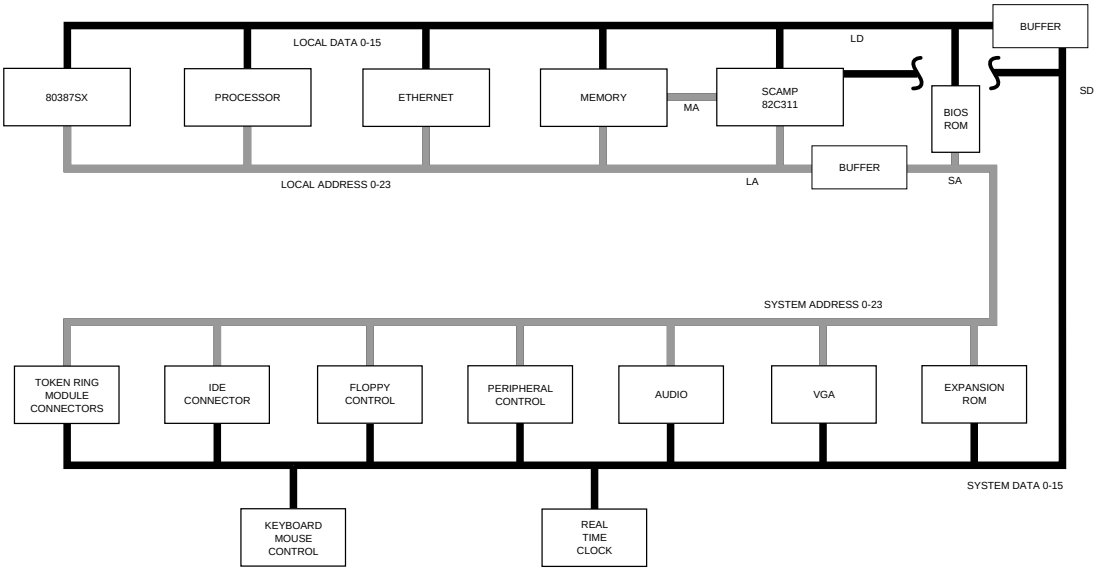
1. Processor: 80386SX
   486SLC
2. 4 Mbytes of RAM
3. 128 Kbyte ROM
4. VL82C311 (SCAMP) AT chipset
5. 8042 keyboard and mouse interface
6. CL-GD542X video controller with 1Mbyte of video RAM
7. 82596SX based Ethernet interface
8. 8051 based LOC Technology security feature
9. ATA compatible hard disk interface
10. 82077 based floppy drive interface
11. 16C452 based serial and parallel ports
12. Four SIMM sockets for memory expansion
13. 146818A Real Time Clock
14. Yamaha YMZ263 based business audio subsystem

The major components are identified in the following illustration.



Description

The following description of the system board should be read in conjunction with the block diagram below. The diagram shows the peripheral areas of circuitry which are connected to the CPU. For clarity, timing and control signals are omitted.



The block diagram is a functional description of the system board and does not identify specific chips.

The LS Pro system board uses highly integrated components, reducing the chip count and the system board area, and increasing reliability. The VLSI SCAMP chipset integrates much of the standard AT system board peripheral logic onto a single chip.

The processor and coprocessor are connected to a 16-bit local bus running at 33MHz. Control logic for the local bus is integrated in SCAMP.

Memory addresses are generated by SCAMP and are routed to system memory on a dedicated memory address bus. Memory data uses the local data bus.

The 82596 based Ethernet interface connects directly to the local bus allowing fast transfers to and from system memory.

The BIOS ROM is addressed from the system bus and places its data on the local bus.

All other peripheral circuitry is connected to the system bus.

Coprocessor

The system board includes a socket for an 80387SX coprocessor. This is a high performance numeric coprocessor which further improves the performance of the processing system in applications which perform many floating point arithmetic operations.

The coprocessor has two I/O ports 00F0h and 00F1h which are used to control reset and error latching. The coprocessor interface control logic is integrated in SCAMP.

If a coprocessor is fitted on the system board it should always be reset at the same time as the processor.

System reset

The system is automatically reset on power up. No external hardware reset facility is provided. Some operating systems provide a software reset e.g. MS-DOS resets the machine if CTRL, ALT and DEL are pressed at the same time.

3.2 PROCESSOR SYSTEM

The processor system uses either an 80386SX or a 486SLC microprocessor, these are described below.

80386SX processor features

The 80386SX is a high performance microprocessor which features:

- 24-bit address and 16-bit data busses.
- compatibility with software written for less powerful members of the 80X86 microprocessor family - the 8086, 8088 and 80286.
- high speed.
- enhanced modes of operation - real, protected and virtual 8086 mode.
- on board memory management unit.

486SLC processor features

The 486SLC incorporates all the features of the 80386SX listed above. In addition it offers:

- 1 Kbyte of cache RAM.
- 80486SX instruction set compatibility.

Address and data bus structure

The system board utilises all address and data lines available on the processor. This allows up to 16 Mbytes of physical memory to be addressed.

The total addressable I/O space of the processor is 64 Kbytes. Section 5 shows how it is used and details the I/O ports used by various devices.

Software compatibility

Existing software which has been written for the 8086/8088/80286 will be executed at greater speed on the 80386SX/486SLC, even higher performance will be achieved with new software which takes advantage of the 80386SX or 486SLC architecture and enhanced instruction set.

Modes of operation

The processor enters real mode at power up or when it is reset. In this mode it provides fast execution in an unprotected mode like that of the 8086 or 80286 in real mode. The main difference between the 80386SX/486SLC, and the 80286/8086 in this mode is speed.

In the protected mode the 80386SX/486SLC has all the advanced architectural features of the 80286: memory management and protection mechanisms, task management, and virtual memory support. In addition it operates with greater speed and supports 32-bit registers and instructions.

In the virtual 8086 mode the 80386SX/486SLC creates one or more 8086 environments within its protected multitask environment. This allows multiple 8086 tasks or a mixture of 8086 and 80286/80386 tasks to be executed concurrently.

3.3 SCAMP

The LS Pro system board is based on a VLSI VL82C311 single chip AT compatible chipset. The VL82C311 integrates the following standard AT system board peripheral logic in a single QFP package:

- two 8237A DMA controllers
- two 82C59A interrupt controllers
- 82C54 system timer
- 74LS612 memory mapper
- 82284 clock generator and ready interface
- 82288 bus controller

In addition to the logic listed above the VL82C311 also includes:

- memory controller
- bus steering logic
- parity generation and checking logic
- Port B and NMI logic

Memory controller

The memory controller integrated in the VL82C311 can access the full 16Mbyte address range of the processor. Memory is addressed in up to four banks of 2 or 8 Mbytes. Page mode operation and interleaving maximise system performance.

Full LIM 4.0 support is included with 36 mapping registers. ROM shadowing is supported from 640k to 1M.

System control port B

Port B is located at I/O location 0061h. The port may be used for: gate timer 2 (speaker); speaker data; RAM parity check enable; enable I/O channel check; refresh detect; timer 2 out; I/O channel check; RAM parity check. The detailed function of each bit is described in section 5.

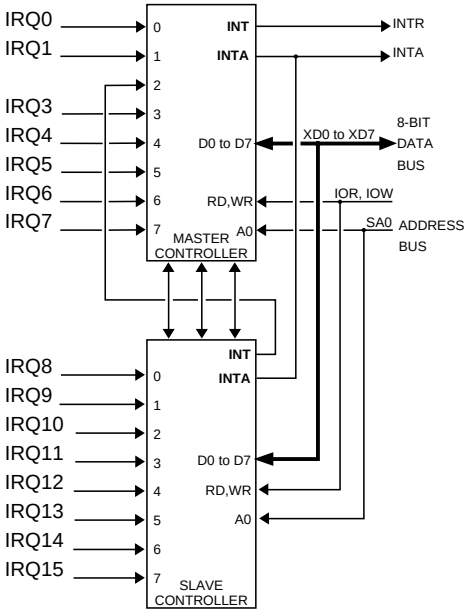
Interrupt structure

The system board supports 16 levels of edge sensitive, maskable hardware interrupts, including Non-Maskable Interrupts (NMI).

The interrupt control circuitry is functionally equivalent to two 8259A programmable interrupt controllers. Each controller has eight interrupt inputs; one interrupt input is used to cascade the controllers together. This leaves fifteen inputs available for the processing system to use.

The output from the controllers goes to the INTR input on the processor. All of the interrupts may be masked using the processor CLI instruction.

The following illustration shows the maskable interrupt structure.



List of hardware interrupts

The interrupts are allocated to hardware functions in the priorities shown in the following table. IRQ0 is the highest priority.

Interrupt level		Function
IRQ0		Timer
IRQ1		Keyboard
IRQ2		Slave controller input
	IRQ8	Real time clock
	IRQ9	Token ring module
	IRQ10	Ethernet port
	IRQ11	Security
	IRQ12	Mouse
	IRQ13	Coprocessor exception
	IRQ14	Hard disk controller
	IRQ15	Digital audio
IRQ3		Reserved
IRQ4		Serial port
IRQ5		Reserved
IRQ6		Floppy disk controller
IRQ7		Parallel port

Note

IRQ0 and IRQ13 are both used inside the SCAMP chip. Neither emerges for use on the system board.

Non-Maskable Interrupts

A non-maskable interrupt (NMI) is generated in the event of a parity or I/O error. Reading Port B indicates the source of the NMI. NMI may be disabled by writing to I/O address 0070h.

On power up, and after a reset the NMI bit of port 0070h is set to 1 (NMI disabled). Before NMI is enabled after a power up the I/O channel check state is initialized by POST.

Note

I/O port 0070h is also used to access the Real Time Clock CMOS RAM, as a result port 0071h must be read immediately after port 0070h has been written to enabling or disabling NMI. If this is not done the successful operation of the Real Time Clock and its CMOS RAM cannot be guaranteed.

Direct Memory Access

Direct Memory Access (DMA) allows data to be transferred to or from system memory without interrupting the system processor. The DMA controller is functionally equivalent to two 8237A DMA controllers.

The DMA controller may be programmed by the system microprocessor. The DMA registers are programmed or read by the system processor addressing the DMA controller in the ranges shown below.

- hex 0000 to 001F
- hex 0081 to 008F
- hex 00C0 to 00DF

Details on the effect and usage of these addresses is given in section 5.

The two 8237A compatible controllers are cascaded with the DREQ and DACK signals of channel 0 on one controller connected to the HRQ and HLDA signals of the other controller. This arrangement results in four 8-bit DMA channels (DMA1) and three 16-bit channels (DMA2).

The table below shows which DMA channels are allocated which functions. DMA channels 0 and 1 support memory-to-memory transfers.

DMA channel	Function
1	Audio
2	Floppy drive interface
3	Audio

Address generation

In order to access the full 16Mbyte address space of the processor the DMA controller must generate a 24-bit address. The bits 0-7 are taken directly from the 8237A address outputs, bits 8-15 are latched from the 8237A data outputs while bits 16-24 are from the appropriate DMA page register.

System timers

The SCAMP chip provides a three channel 82C54 compatible system timer. The counters are:

counter 0 system timer

counter 1 refresh request

counter 2 sound output

Full details on the operation of 8254 counters are given in the manufacturers data sheets and are not repeated here.

The system timers are programmed by accessing the four I/O ports recognised by the timers. The counters provide six modes of operation. The four I/O ports which are used to program the counters are organised as one count register for each counter and one control byte (I/O ports 0040h to 0043h). The function of each port is given in section 5.

Operation

The clock input to the timer is 1.193 MHz. This is obtained by dividing the14.31818 MHz system oscillator (OSC) by twelve. The output frequency of each timer is then separately programmed by loading the associated count register.

System timer

BIOS loads the counter 0 registers with a value of 65536 which results in a system timer frequency of approximately 18.2Hz. The output of counter 0 generates a hardware interrupt, IRQ0, which is used to maintain a time of day clock based on the number of "ticks" since midnight.

Refresh request

The BIOS loads the counter 1 registers with a value of 18 which generates a refresh request rate of 66.278kHz (one refresh request every 15.08 µseconds). A refresh request puts the processor into hold and accesses memory via a DMA type operation.

Sound output

The sound output may be set to give the output frequency required. To enable the output bit 0 of Port B (I/O 0061h) must be set to 1.

3.4 SYSTEM MEMORY

General

The system board contains:

- 128 Kbytes of ROM.
- system RAM.
- 50 byte battery backed Real-time clock CMOS RAM.
- expansion ROM socket (optional).

Read only memory (ROM)

The system ROM contains the BIOS and the system board Setup utility. It consists of a 1 Mbit EPROM arranged as 128 Kbytes of memory. It is addressed at the top of the first and last Megabyte of the processor address space and is not parity checked.

The lower 64 Kbytes of the ROM contains code which is used only during the boot process. If shadow RAM is enabled this lower 64 Kbyte address space (E0000-EFFFF) is available for use as RAM. If shadowing is disabled the top 128 Kbytes of the first and last Mbytes are used by the system ROM.

Random access memory (RAM)

Four Megabytes of RAM are soldered directly to the system board. Additional RAM is plugged into SIMM sockets on the system board. Upgrades are in pairs of 1 or 4 Mbyte SIMMs giving upgrade capacities of 2 and 8 Mbytes. The following table gives the permissible upgrade combinations and the total system RAM available with each.

System board capacity (Mbytes)	Upgrade to (Mbytes)	Bank (Mbytes)		
		1	2	3
4	6	N/A	2	-
4	8	N/A	2	2
4	12	N/A	8	-
4	16	N/A	8	8

Note

When banks 2 and 3 are both occupied by 8 Mbyte upgrades the RAM soldered to the system board is disabled.

Real time clock (RTC) RAM

The real time clock and its associated battery backed RAM is an MC146818. The RTC RAM is accessed via I/O ports 0070h and 0071h. The first fourteen bytes are used to store real time clock information, the remainder are used for system configuration data.

The RTC is normally powered from the system +5V supply. However when the computer is not switched on power is supplied by a rechargeable battery on the system board. This maintains the correct time and configuration information. If the battery becomes discharged the time and date will need to be reset and the system will need to be reconfigured using the SETUP utility.

Contents of RTC RAM

The contents of the RTC RAM are listed below.

Address	Function	Address	Function
Real time clock data		16	Base memory (high byte)
00h	seconds	17	Expected expanded memory (low byte)
01h	alarm seconds	18	Expected expanded memory (high byte)
02h	minutes	19	Drive type for hard drive 0
03h	alarm minutes	1A-1E	Reserved
04h	hours	1F	shadow BIOS
05h	alarm hours	20-27	Reserved
06h	day of week	28	Apricot sound volume
07h	date	29	Apricot options
08h	month	2A	Apricot boot type
09h	year	2B	Apricot cache disable (see also byte 34h)
0Ah	status register A	2C-2D	Reserved
0Bh	status register B	2E	High byte checksum for 10-2D
0Ch	status register C	2F	Low byte checksum for 10-2D
0Dh	status register D	30	Actual expanded memory (low byte)
0E	Diagnostic Status	31	Actual expanded memory (high byte)
0F	Shutdown code	32	Century in BCD
Configuration data		33	Memory exceeds 512K/387 presence
10	Diskette drive type	34	486SLC cache control (see also Apricot byte 2Bh)
11	Reserved	35	Apricot access rights
12	Fixed disk drive type	36	Floppy/Token-Ring autodetect
13	Power on password	37	Hard disk autodetect
14	Equipment byte	38-3E	Power on password
15	Base memory (low byte)	3F	Byte checksum of bytes 38-3E

The contents of each of the RTC RAM locations which requires further explanation is described in the following table.

Location/Title	Bit(s)	Function
0E	7	1 = Real time clock lost power
Diagnostic	6	1 = CMOS checksum bad
status	5	1 = Invalid configuration at POST
	4	1 = Memory size error at POST
	3	1 = Fixed disk fails initialization
	2	1 = CMOS time found invalid
	1, 0	Reserved
0F	7-0	00h = Normal execution of POST
Shutdown		01h = Chipset initialization for real mode re-entry.
code		05h = Issue an EOI and JMP to 40:67h
		06h = JMP to 40:67h without an EOI
		07h = Return to INT 15h function AH=87h block move
		08h = Return to POST memory test
		09h = Return to INT 15h function AH=87h block move
		0Ah = JMP to 40:67h without an EOI
10	7-4	Drive type of diskette drive 0
Diskette		0000 = No drive
drive type		0001 = Not used (360k)
		0010 = Not used (1.2MB)
		0011 = Not used (720k)
		0100 = 1.44MB
		0101-1111 are Reserved
	3-0	Reserved (no second drive)
12	7-4	Drive type for drive 0 (0-14) if 15 look at byte 19h
Fixed disk	3-0	Reserved
drive type		
13	7-1	Reserved
Power on	0	1 = Power on password enabled
password		
14	7-6	Diskette drives installed
Equipment		00h = 1
byte		01-03h Reserved
	5-4	Primary display adapter
		00h = VGA
		01h = Not used (40 column colour)
		02h = Not used (80 column colour)
		03h = Not used (Monochrome)
	3-2	Reserved
	1	1 = 80387 installed
	0	1 = Diskette drive available for boot

Location/Title	Bit(s)	Function
1F	7-4	Reserved
Shadow BIOS	3	1 = shadow BIOS
	2-0	Reserved
28	7-0	Sound volume 0 = minimum, FF = maximum
Sound volume		
29	7	1 = Power on sound enabled
Options	6	1 = Quiet boot (No text output)
	5	1 = Fast boot
	4-3	Reserved
	2	1 = Graphical boot
	1-0	Monitor type
		00 = VGA
		01 = HiVision 14"
		10 = HiVision Low Emission
		11 = Reserved
2A	7	Token-Ring Bus width (see 36h bit 1)
Boot type		1 = 16-bit, 0 = 8-bit
	6	Token-Ring data rate
		0 = 16 Mbits/sec, 1 = 4 Mbits/sec
	5	1 = Token-Ring present
	4-3	Reserved
	2-0	Remote Boot type
		000 = None
		001 = Ethernet RPL
		010 = Token-Ring RPL
		100 = Optional ROM at C000
2B	7-0	00h = Cache enabled
Cache disable		CDh = Cache disabled (see 34h)
33	7	1 = memory exceeds 512K
RAM exceeds	6-5	Reserved
512K/387 status	4	Save 387 status
		1 = present, 0 = not present
	3-0	Reserved
34	7-6	Reserved
486SLC cache	5	1 = cache enabled (see 2Bh)
	4-0	Reserved
35	7-2	Reserved
Access rights	1	1 = Setup access right enabled
	0	1 = Floppy boot right enabled
36	7-2	Reserved
Floppy/	1	1 = Token-Ring present
Token-Ring	0	1 = Floppy drive present
autodetect		

3.5 VIDEO ADAPTER

General

The video adapter on the LS Pro system board is based on either a Cirrus Logic CL-GD5422 or 5426 chip. These chips contain all the elements of a VGA controller, except display memory, providing 100% compatibility with the IBM VGA standard.

The video controller consists of the GD542X, 1 Mbyte of display memory and a 7.6mA current reference. Video dot clocks vary from 25 to 65 MHz depending on video mode.

Software support is provided by a video BIOS included in the system BIOS.

In addition to full compatibility with the VGA standard the video controllers support a range of enhanced video modes.

The video modes available are given in the following table:

Mode	Type	Colours	Displayed Chars	Character Cell	Pixels
0, 1	Text	16/256K	40x25	9x16	360x400
2, 3	Text	16/256K	80x25	9x16	720x400
4, 5	Graphics	4/256K	40x25	8x8	320x200
6	Graphics	2/256K	80x25	8x8	640x200
7	Text	-	80x25	9x16	720x400
D	Graphics	16/256K	40x25	8x8	320x200
E	Graphics	16/256K	80x25	8x8	640x200
F	Graphics	-	80x25	8x14	640x350
10	Graphics	16/256K	80x25	8x14	640x350
11	Graphics	2/256K	80x30	8x16	640x480
12	Graphics	16/256K	80x30	8x16	640x480
13	Graphics	256/256K	40x25	8x8	320x200
58	Graphics	16/256K	100x37	8x16	800x600
5C	Graphics	256/256K	100x37	8x16	800x600
5D	Graphics	16/256K	128x48	8x16	1024x768
5F	Graphics	256/256K	80x30	8x16	640x480
60	Graphics	256/256K	128x48	8x16	1024x768
64	Graphics	64K	-	-	640x480
65	Graphics	64K	-	-	800x600
66	Graphics	32K	-	-	640x480
67	Graphics	32K	-	-	800x600
6C	Graphics	16/256K	160x64	8x16	1280x1024
6F	Graphics	64K	40x25	8x8	320x200
70	Graphics	16M	40x25	8x8	320x200
71	Graphics	16M	80x30	8x16	640x480

Note

Mode 6C is interlaced only.

Sync signals output to the monitor are at TTL levels while the analogue video outputs are at 0 to 0.7 volts.

Video controllers

The video controllers implement all the control and data registers, and all the data manipulation capabilities and data paths of the standard VGA controller. In addition they can generate high-resolution display modes (those supported in BIOS are listed in the table above), and uses several enhancements to improve on the performance of the standard VGA implementation.

These enhancements include a pair of FIFOs. One isolates the processor from display memory, allowing zero wait state writes from processor to display memory, provided the FIFO is not full. Reads also occur with zero wait states provided the data required is held in the FIFO. The second allows the use of fast page mode cycles to fetch data from display memory, increasing the time that the display memory is available for processor accesses.

In addition the GD5426 includes a hardware BitBLT which accelerates video performance under GUIs.

3.6 FLOPPY DISK CONTROLLER

General

The diskette drive controller fitted on the system board is an Intel 82077 chip. This single chip provides a complete IBM compatible floppy disk controller, including data separator, on a single chip.

The controller has several internal registers which are accessible by the system microprocessor. These registers, and their usage, are described in detail in section 5. An illustration and pinout of the floppy drive connector are given at the rear of this section.

Drive formats

The controller supports:

- two drives
- 500 kbyte unformatted media, 360 kbyte formatted
- 1 Mbyte unformatted media, 720 kbyte formatted
- 1.66 Mbyte unformatted media, 1.2 Mbyte formatted
- 2 Mbyte unformatted media, 1.44 Mbyte formatted
- supports 250, 300 and 500 kbits/sec transfer rates
- programmable precompensation delay

In this implementation a single 1.44 Mbyte floppy drive can be fitted. 720k and 1.44M diskettes are supported for both single and multithread operations. The default precompensation is 125 nanoseconds and is present for all cylinders.

3.7 HARD DISK INTERFACE

General

The hard disk drive connector which is fitted on the LS Pro system board is an IDE connector which conforms to the ATA interface standard.

The hard disk drive is accessed via a group of I/O ports at 01F0-01F7h. The function of each port is given in section 5.

The connector is buffered from the system bus by bi-directional transceivers. A pinout of this and the hard disk drive power connector is given at the rear of this section.

Interface signal descriptions

Host reset

Reset signal to the drive. Active low during system power up.

Host data 0-15

16-bit bi-directional data bus between the system board and the drive.

Host I/O channel ready

This line allows the drive to lengthen I/O read and write cycles by generating system board wait states. The signal is normally high and is driven low by the drive if an I/O cycle is to be lengthened.

Host IOW

Write strobe. This signal clocks data from the system board to the drive on the data bus.

Host IOR

Read strobe. This signal clocks data from the drive to the system board on the data bus.

Host IRQ14

This is the interrupt signal from the drive. This signal is active high when the drive is selected and the drive interrupt enable bit (IEN) is activated by the system board. An interrupt is cleared when the drive receives the next command, when the drive status register is read, or when the drive is reset.

Host IOCS16

Informs the system board that the drive data register has been enabled and the drive is prepared to perform a 16-bit I/O transfer.

Host ADDR 0-2

These lines are used to select registers on the drive.

3.8 PERIPHERALS CONTROLLER

A 16C452 peripherals controller provides two serial and one parallel port.

Serial ports

The serial controllers integrated in the 16C452 are fully compatible with the NS16450 serial communications controller. They automatically add and remove start, stop and parity bits. Programmable baud rate generators allow operation from 50 baud to 56 Kbaud. The ports support 5, 6, 7 and 8-bit characters with 1, 1.5 or 2 stop bits. A prioritized interrupt system controls transmit, receive, error and line status as well as data-set interrupt.

Each serial port controller provides the following functions:

- Full double buffering in character mode
- False start-bit detection
- Line-break generation and detection
- Modem control functions:
  - Clear to send (CTS)
  - Request to send (RTS)
  - Data set ready (DSR)
  - Ring indicator (RI)
  - Data carrier detect (DCD)

Note

The DSR, DTR and RI modem control signals of COM2 do not appear on the serial port at the rear of the system unit.

COM1 is connected to the system address and data busses using IRQ4 while COM2 uses IRQ3. The controllers occupy a group of eight consecutive I/O ports COM1 at 03F8-03FFh and COM2 at 02F8-02FFh. The ports have the following significance.

Location	Significance
0	Transmit Data
	Receive Data
	Baud Rate Generator Divisor (Low byte)
1	Baud Rate Generator Divisor (High byte)
	Interrupt Enable
2	Interrupt Identification Register
3	Line Control Register
4	Modem control Register
5	Line Status Register
6	Modem Status Register
7	Scratch Pad Register

Programmable baud-rate generator

The serial port controllers each contain a programmable baud-rate generator which can divide the clock input (1.8432 MHz) by any divisor from 1 to 65,535. The output frequency of the baud-rate generator is the baud-rate multiplied by 16. Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during setup to ensure the correct operation of the baud-rate generator. When either of the divisor latches is loaded, a 16-bit baud counter is immediately loaded. This prevents long counts on the first load.

Parallel port

The parallel port is fully compatible with the IBM AT parallel port. The port is output only and allows the attachment of peripherals that accept parallel data at standard TTL levels.

A pinout and illustration of parallel port 25-pin D-shell connector is given at the rear of section 2.

The parallel port is accessed via the three I/O ports given in the following table.

Address	R/W	Function
03BCh	r/w	Data register
03BDh	read	Status register
03BEh	write	Control register

These registers control the operation of the parallel port. They are described in detail in section 5.

3.9 KEYBOARD/MOUSE CONTROLLER

General

The keyboard and mouse interfaces are implemented on the system board on an Intel 8042 chip. The keyboard connector on the system unit is dedicated to that function, the mouse connector can be used for any auxiliary device with a serial interface compatible with the 8042. Illustrations and pinouts of these connectors are at the rear of section 2.

The 8042 receives the serial data, checks the parity, translates the keyboard scan codes and presents the data to the system as a byte of data at data port I/O address 0060h. The interface can interrupt the system when data is available or can wait for polling from the microprocessor.

I/O address 0064h is the command/status port. When the system reads port 0064h it receives status information from the 8042. When the system writes to the port, the 8042 interprets the byte as a command.

The significance of port 0064h is described in section 5.

Keyboard password security

The 8042 provides a password security mechanism. Three commands are available regarding password operation:

A4 Test Password Installed

A5 Load Security

A6 Enable Security

The system microprocessor may determine if a password is currently installed with a Test Password Installed command. This allows a controlling program to decide whether or not to overwrite an existing password.

The system microprocessor may set a password in the 8042 at any time with a Load Security command. Any existing password is lost, and the new password becomes the active password. The password must be installed in scan code format.

The system microprocessor places the system in secure mode with the Enable Security command. In secure mode the 8042 does not pass any information to the system microprocessor. The 8042 intercepts the keyboard data stream and continuously compares it with the installed password pattern. No keyboard or auxiliary device data is passed to the system microprocessor until a match is found. When a match occurs the 8042 is restored to its previous state and data is passed to the system microprocessor.

There is no limit to the number of times the password may be changed. No command is available to verify the installed password. The 8042 accepts no commands when keyboard security is active.

3.10 LOC TECHNOLOGY

The system board is fitted with a LOC Technology security subsystem. This subsystem allows Apricot LOC Technology software to control access to data and facilities.

When Apricot LOC Technology is not in use the security hardware is passive and has no effect on the system.

3.11 ETHERNET PORT

General

The Ethernet port on the system board is based around an 82596 Local Area Network Coprocessor, an 82C503 Dual Serial Transceiver and an AMD7997. This provides a port which complies fully with the IEEE 802.3, 10BASE5, 10BASE2 and 10BASET specifications.

The coprocessor and dual serial transceiver make up an Ethernet controller for thick cabling, and with an additional analog filter module a TPE controller. The 7997 interfaces between the thick and thin Ethernet cabling standards.

An expansion ROM socket may be fitted to the system board. This socket is intended to allow for alternative remote boot ROMs. The system BIOS includes RPL remote boot code.

The Ethernet standard defines a requirement for every device to have a unique address. This is implemented in a PROM on the system board.

The Ethernet port occupies a group of 17 I/O ports. The ports have the following significance:

Location (Hex)	Significance
0	Port
1-3	Reserved
4	CA
5-7	Reserved
8-D	Ethernet Address
E	Reserved
F	Checksum
10	Status register

82596 LAN coprocessor

The 82596 is connected to the processor local bus. The 82596 is an intelligent co-processor which performs many network control tasks.

The inherent intelligence of the 82596 reduces host processor overhead, and allows all time critical functions to be performed independently of the host. This along with the inherent speed of the processor local bus results in a high performance network interface, with minimum host processor overhead.

The host processor monitors and controls the 82596 through a shared memory structure known as the System Control Block (SCB). The 82596 uses the HOLD and HOLDA signals to gain control of the local bus in order to access the SCB.

Both the 82596 and the host can modify the SCB. The processor uses the Channel Attention (CA) line to notify a change to the 82596, while the 82596 generates a hardware interrupt if it has modified the SCB.

The host can communicate with the 82596 via a single port (PORT). This allows the host to, amongst other things, reset the 82596.

Full details on the 82596 and its operation are given in the manufacturers data sheets.

82C503 dual serial transceiver

The 82503 dual serial transceiver (DST) incorporates all the active circuitry necessary to interface the 82596 to an AUI port and a TPE network. In addition to the normal features of an IEEE 802.3 transceiver the 82503 also incorporates automatic port selection, and polarity switching.

Automatic port selection selects either TPE or the AUI port without external intervention. If a good TPE connection is available the 82503 will select the TPE port, if no TPE connection is available the AUI port will be selected.

Note

The thin cable Ethernet port is derived from the AUI port. To select thick or thin Ethernet, SW1 must be in the correct position.

Automatic polarity selection allows the 82503 to overcome the most common wiring problem on TPE networks. If the polarity of the receive signal pair is reversed as a result of a crossed pair of wires, the 82503 automatically corrects the error by reversing the signals internally.

7997

The Ethernet transceiver chip acts as the interface between thick and thin Ethernet cabling standards, implementing the IEEE802.3 10BASE2 standard.

3.12 APRICOT BUSINESS AUDIO

The Apricot Business Audio subsystem integrated on the LS Pro system board is based on a Yamaha YMZ263 chip. It offers two channels each of which can be independently configured to either playback or record.

Each channel incorporates a PCM/ADPCM encoder/decoder, 12-bit ADC and DAC and a 128 byte FIFO. In PCM mode the maximum sample rate is 44.1kHz, in ADPCM it is 22.05kHz.

The digital audio subsystem uses DMA channel 1 to transfer data to and from audio channel 0 and DMA channel 3 for audio channel 1.

The YMZ263 occupies a block of eight ports from 388-38Fh. A description of the operation of this block of ports is included section 5.

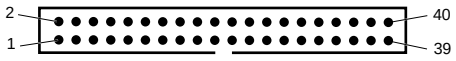
3.13 SYSTEM BOARD CONNECTORS

Hard disk drive connectors

Control Connector

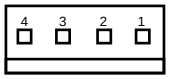
Pin	Function	Pin	Function
1	host reset-	21	-
2	ground	22	ground
3	host data 7	23	host IOW-
4	host data 8	24	ground
5	host data 6	25	host IOR-
6	host data 9	26	ground
7	host data 5	27	host I/O channel ready-
8	host data 10	28	-
9	host data 4	29	reserved
10	host data 11	30	ground
11	host data 3	31	host IRQ14
12	host data 12	32	host IOCS16-
13	host data 2	33	host ADDR1
14	host data 13	34	-
15	host data 1	35	host ADDR0
16	host data 14	36	host ADDR2
17	host data 0	37	-
18	host data 15	38	-
19	ground	39	-
20	key	40	ground

The pin layout of the connector.



Power connector

Pin	Function
1	+12 Volts
2	ground (for +12V)
3	ground (for +5V)
4	+5 Volts

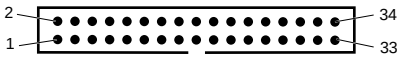


Floppy drive connector

Pin	Function	Pin	Function
2	density select 1	14	drive select 2
3	not connected	16	motor on
4	not connected	18	direction
5	5V	20	step
6	density select 0	22	write data
7	5V	24	write enable
8	index	26	track 00
9	5V	28	write protect
10	drive select 0	30	read data
11	5V	32	head select
12	drive select 1	34	disk change

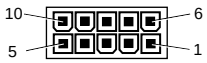
Note

All other pins are connected to 0 Volts.



System board power connector

Pin	Function
1	+12V
2	+12V
3	+5V
4	+5V
5	0V
6	0V
7	0V
8	0V
9	-12V
10	Power good



Battery jumper

A two position jumper is provided alongside the system board battery. With the jumper in the position away from the power supply metalwork the battery provides power to the system board maintaining the contents of CMOS RAM and powering the Real time clock when mains power is not available.

If the jumper is moved to the position nearest the power supply metalwork battery power to the system board is disconnected, and the CMOS RAM is discharged.

The jumper is identified in the illustration on page 2/5, and instructions on accessing the system board are given in section 2.

Contents

4.1 POWER SUPPLY

Description

The power supply is an extremely compact unit which fits inside the system unit and provides DC power for the system unit and an AC outlet to power a monitor. The unit contains: mains inlet and outlet, voltage selection jumper, DC power outlet for the system board and power outlet for the system unit fan.

The power supply is designed to meet international safety standards.

Mains input to the power supply is at the rear of the PSU via a 3-pin AC inlet. Alongside the input connector is an auxiliary 3-pin outlet which supplies power to a monitor. A single low voltage output cable harness supplies power within the system unit. A two pin connector on the power supply PCB provides power for the system unit fan.

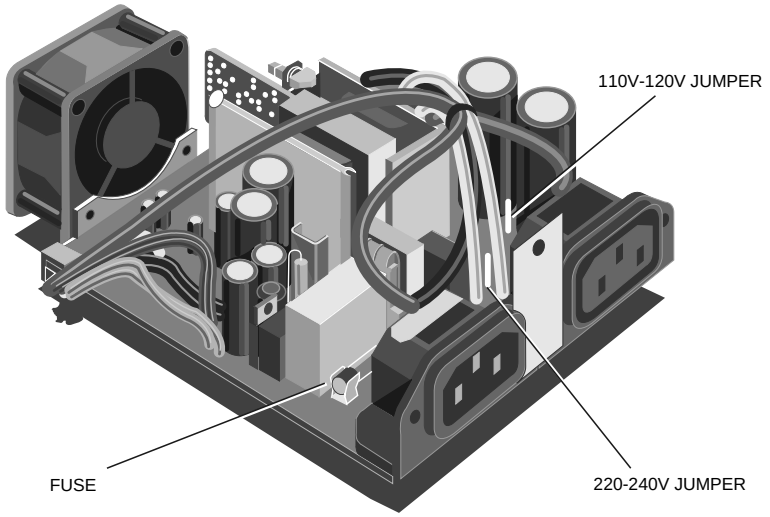
Warning

The auxiliary AC outlet must only be used to power monitors approved by Apricot.

The power supply on/off switch acts as the system on/off switch and is operated from the front panel via a mechanical linkage.

The unit generates an active high Power good signal which is only taken high after the DC outputs are stabilised. The signal goes low at least 1mS before the DC outputs fall outside specification. This signal is used to disable read and write operations to the RTC, battery backed RAM and the Security RAM before power is removed.

The power supply unit is shown in the following illustration.



The unit can accept power from either 110-120V or 220-240V AC supplies. The input voltage is selected by a jumper on the power supply PCB. The location of the jumper is shown in the illustration above.

An internal 4A 250V (T4H) fuse is fitted in the power supply. In the event of a failure only replace the fuse with one of the same type and rating. Determine the cause of the failure before replacing the fuse.

Note

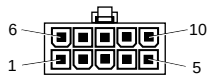
If the PSU is dismantled it must be subjected to the following electrical safety tests before being returned to service:

1. *Earth bond continuity*
2. *Insulation resistance*
3. *Dielectric strength*
4. *Earth leakage*

Connector

The voltage output cable is terminated in a ten way plug. The pinout and connector details are given below.

Pin	Function
1	+12V
2	+12V
3	+5V
4	+5V
5	0V
6	0V
7	0V
8	0V
9	-12V
10	Power good



4.2 MONITORS

Introduction

Apricot supplies 14" colour SVGA, and 14" and 17" colour EVGA monitors. All Apricot SVGA and EVGA monitors described here are low emission monitors which are compliant with the MPR2 radiation legislation.

These monitors are fully compatible with the adapter on the system board and may be used in any standard VGA display mode. Standard VGA display modes include:

640 pixel x 480 line (VGA mode)
640 pixel x 400 line (CGA double line mode)
640 pixel x 350 line (EGA mode)
720 pixel x 350 line (MDA mode)

In all the modes given above the monitors display 80 columns x 25 rows of characters, but the character cell size varies from mode to mode as follows:

8 x 19 (VGA mode)
9 x 16 (VGA mode)
8 x 14 (EGA mode)
8 x 16 (CGA double line mode)
9 x 14 (MDA mode)

SVGA monitors can also display higher resolution video signals of 800 pixels x 600 lines non-interlaced, and 1024 pixels x 768 lines interlaced. EVGA can display higher resolution video signals of 800 pixels x 600 lines, and 1024 pixels x 768 lines non-interlaced

This section describes the monitors and gives brief servicing information. The procedures described here do not cover in-depth fault finding and repair but are intended to provide maintenance personnel with basic setting-up procedures.

Important - Safety precautions

When performing any adjustment on a monitor, remember that the unit contains lethal voltages. As the setting-up adjustments must be performed with the power on, these adjustments must only be carried out by qualified personnel and great care should be exercised at all times.

Maintenance

Occasionally it may be necessary to clean the screen or cabinet of your monitor. Before cleaning, check that the system is turned off and that the monitor is disconnected from the mains outlet. After cleaning, check that the monitor is completely dry before it is reconnected and turned on.

To clean the screen:

Turn the monitor off. Wet a soft cloth with water, wring the cloth almost dry and wipe the screen. To prevent streaking, do not wipe the screen dry, allow it to dry naturally.

To clean the cabinet:

Turn the monitor off. Clean the cabinet with a soft cloth and a small amount of mild detergent solution. Rinse the cloth with clean water and then wipe the cabinet to remove any detergent residue. Clean the bezel area in the same manner.

Refer any other maintenance problems to a qualified service technician. These products contain no user-serviceable or replaceable parts.

Video signal

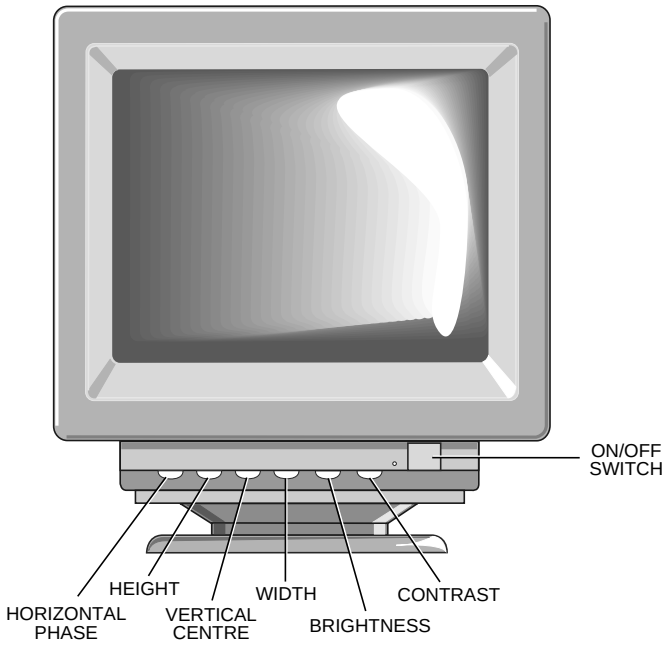
All the Apricot monitors can be used with any computer which supplies an analogue video signal with a 31.47kHz horizontal scan frequency. Because the monitors accept analogue video signals, an infinitely variable range of gray shades/colours may be displayed. The actual number of gray shades/colours is limited only by the video source supplying the signal.

Apricot SVGA colour monitor

The Apricot SVGA colour monitor supports 800x600 (SuperVGA) non-interlaced and 1024x768 (8514/A) interlaced outputs in addition to all standard VGA modes.

External controls All external controls are on the front of the monitor. In addition to the power switch there are: contrast, brightness, width, vertical centre, height and horizontal phase controls.

The following illustration shows the controls.



Power switch

Select the 'O' position to turn the monitor off.

Select the 'I' position to turn the monitor on.

Contrast

This control varies the difference in intensity between the black and white areas of the display.

Brightness

This control varies the average intensity of illumination of the display, and should be set to give the required level of brightness.

Note

Avoid setting the brightness and contrast controls for an excessively bright display. If such a display is left on the screen for an extended period the screen phosphor may be damaged.

Width

This control adjusts the overall width of the on screen image.

Vertical centre

This control adjusts the vertical position of the display area.

Height

This control adjusts the overall height of the on screen image, and only affects the 800x600 display mode.

Horizontal phase

This control adjusts the horizontal position of the display area, and only affects the 800x600 and 1024x768 display modes.

HiVision Low Emission 14" colour

The HiVision 14" Low Emission colour monitor is an EVGA monitor that supports four horizontal sync (31.5, 35-38, 48 and 57 kHz) and three vertical sync frequencies (60, 70 and 72 Hz). All VGA display modes are supported plus 800x600 and 1024x768 resolutions.

External controls

On the front of the monitor are the power switch and brightness and contrast controls.

The following illustration shows the controls on the front of the monitor.

Power switch

Select the 'O' position to turn the monitor off.

Select the 'I' position to turn the monitor on.

Brightness

This control varies the average intensity of illumination of the display, and should be set to give the required level of brightness.

Contrast

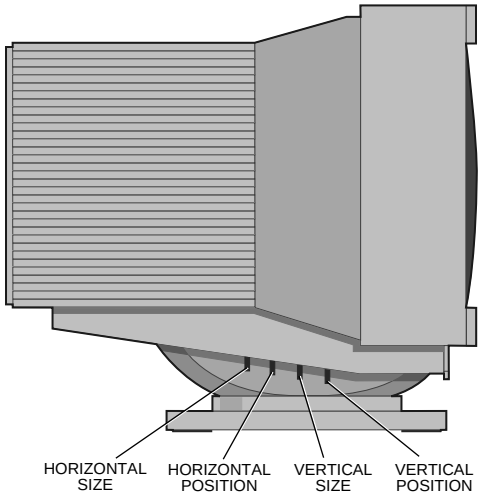
This control varies the difference in intensity between the black and white areas of the display.

Note

Avoid setting the brightness and contrast controls for an excessively bright display. If such a display is left on the screen for an extended period the screen phosphor may be damaged.

On the left side of the monitor are horizontal and vertical size and position controls.

The following illustration shows the controls on the left side of the monitor.



Horizontal size

This control adjusts the overall width of the on screen image.

Horizontal position

This control adjusts the horizontal position of the display area.

Vertical size

This control adjusts the overall height of the on screen image.

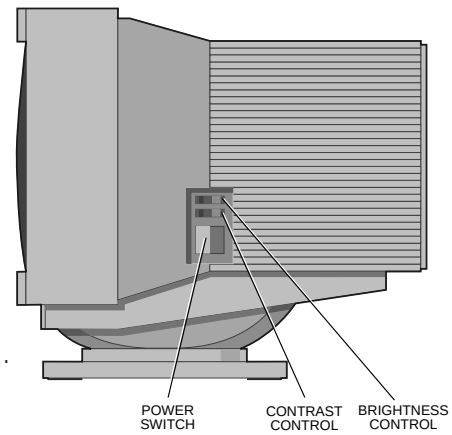
Vertical position

This control adjusts the vertical position of the display area.

HiVision Low Emission 17" colour

The HiVision 17" Low Emission colour monitor supports four horizontal sync (31.5, 35-38, 48 and 57 kHz) and three vertical sync frequencies (60, 70 and 72 Hz). All VGA display modes are supported plus 800x600 and 1024x768 resolutions.

External controls On the right side of the monitor are the power switch and brightness and contrast controls. These are shown in the following illustration.



Power switch

Select the 'O' position to turn the monitor off.

Select the 'I' position to turn the monitor on.

Brightness

This control varies the average intensity of illumination of the display, and should be set to give the required level of brightness.

Contrast

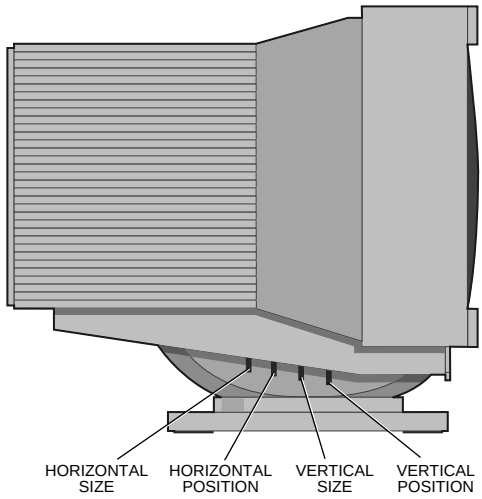
This control varies the difference in intensity between the black and white areas of the display.

Note

Avoid setting the brightness and contrast controls for an excessively bright display. If such a display is left on the screen for an extended period the screen phosphor may be damaged.

On the left side of the monitor are horizontal and vertical size and position controls.

The following illustration shows the controls on the left side of the monitor.



Horizontal size

This control adjusts the overall width of the on screen image.

Horizontal position

This control adjusts the horizontal position of the display area.

Vertical size

This control adjusts the overall height of the on screen image.

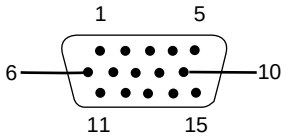
Vertical position

This control adjusts the vertical position of the display area.

VGA Connector

The monitors are connected to the system board video adapter via a 15 pin D-type connector. The pinout and details are given below.

Pin	Signal
1	Red
2	Green
3	Blue
4	Reserved
5	Self test
6	Red rtn
7	Green rtn
8	Blue rtn
9	Plug
10	Digital G
11	Reserved
12	Reserved
13	Hsync
14	Vsync
15	Reserved



4.3 HARD DISK DRIVES

Introduction

Four capacities of hard disk drives are available for the Apricot LS Pro range. All the drives are 1" high, 3.5" form factor using an ATA compatible IDE interface.

The 85,127 and 170 Mbyte drives are from the Quantum ProDrive ELS range, the 213 Mbyte drive is a Maxtor 7213A, the 240 Mbyte drive is a Quantum LPS240A and the 525 Mbyte drive is a Quantum LPS 525A.

Drives connect to the system board hard disk drive connector via a 40-way ribbon cable. Power is supplied via a separate power connector linked to the system board.

Registers The system board accesses hard disk drives in I/O space via registers in locations 01F0h to 01F9h. The function of these registers and their bit significance is given in section 5.

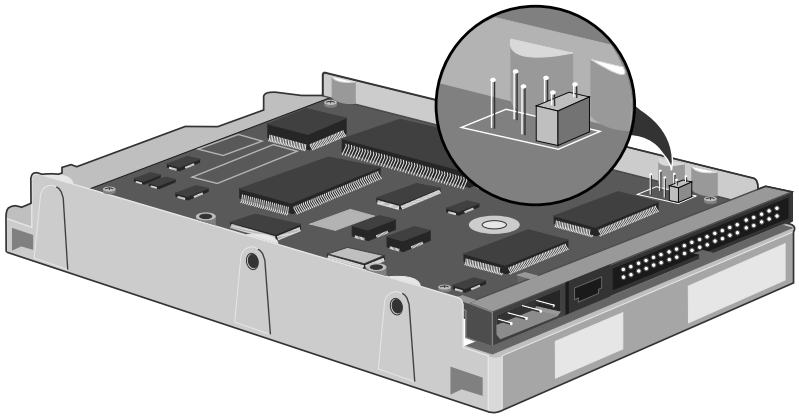
Quantum ProDrive ELS

The 85, 127 and 170 Mbyte hard disk drives that may be fitted in the LS Pro range are from the Quantum ProDrive ELS range. The drives have nominal access times of 17mS and can transfer data at up to 4.0 Mbytes per second.

The drive circuit board contains the drive control electronics and a hard disk controller. A preamplifier for the read/write circuitry and an optical encoder are located underneath the drive cover.

The drives feature an on-board media defect and error recovery scheme which is fully user transparent.

Jumpers Three jumpers on the drive circuit are used to configure the drive. These are shown, properly configured, in the following illustration.



The three jumpers are labelled DS (Drive select), CS (Cable select) and SP (Slave present). The DS jumper must be fitted and the CS and SP jumpers not, in order for the drive to function in an LS Pro.

Drive formats The following table shows the physical format of the drives:

Drive	85	127	170
Disks	1	2	2
Heads	2	3	4
Tracks	3056	4584	6112

Formatting

These drives are low level formatted during manufacture. This format has been optimized to allow the drive to provide maximum performance. Standard low level formatting programs can only reduce the performance of the drive.

Warning

Do not attempt to perform a low level format on a ProDrive, this can only adversely affect the performance of your drive. If you do try to format your drive most standard low level formatting programs will return a "Drive formatted" message very quickly. In fact, the drive has not been formatted.

Discache The Quantum ProDrive ELS drives are fitted with 32kbytes of RAM and look-ahead cache circuitry known as Discache.

When a read access is made to the drive, Discache loads subsequent data into the RAM. If an attempt is made to read this data it is accessed from RAM rather than from the disk, thus considerably reducing access times.

Cache performance benefits tend to be application dependent. Discache has a number of alterable parameters which allow the cache to be configured for maximum performance benefit in any given application.

Full information on configuring Discache is given in the Quantum specification.

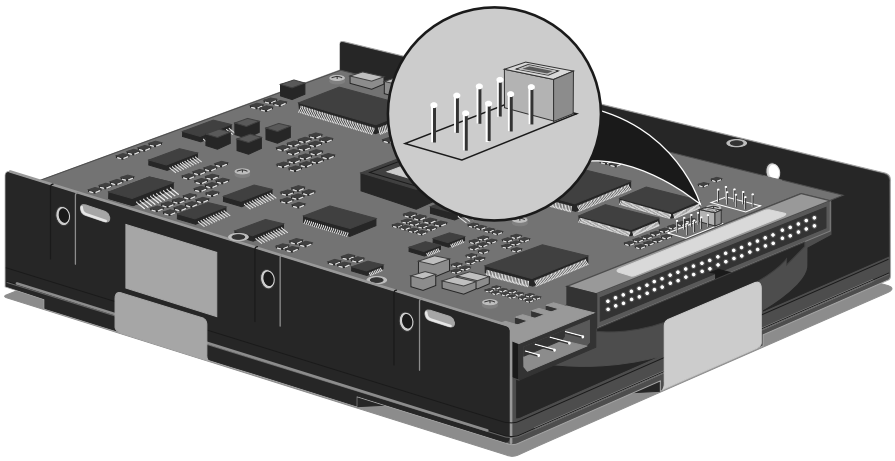
Maxtor 7213A

The 213 Mbyte hard disk drive that may be fitted in the LS Pro range is a Maxtor 7213A. It has a nominal access time of 15mS and can transfer data at up to 8.0 Mbytes per second.

The drive circuit board contains the drive control electronics and a hard disk controller. A read preamplifier and the write drive circuitry are located underneath the drive cover.

The drive features an on-board media defect and error recovery scheme which is fully user transparent.

Jumpers Nine jumpers on the drive circuit are used to configure the drive. These are shown, properly configured, in the following illustration.



The jumpers are labelled J16 to J20 and J22 to J25. In the LS Pro application only J20 should be fitted. If J20 is not fitted or if any of the other jumpers are fitted the drive is unlikely to operate correctly.

Drive format The drive has two disks and four data surfaces, and features a Universal Translate Mode which allows it to be configured with any combination of cylinders, heads and sectors within the drive's formatted capacity.

Formatting

These drives are low level formatted during manufacture. This format has been optimized to allow the drive to provide maximum performance. Standard low level formatting programs can only reduce the performance of the drive.

> **Warning**
>
> *Do not attempt to perform a low level format, this can only adversely affect the performance of your drive. If you do try to format your drive most standard low level formatting programs will return a "Drive formatted" message very quickly. In fact, the drive has not been formatted.*

Cache The drive is fitted with 64kbytes of RAM and read-ahead cache circuitry.

When a read access is made to the drive, subsequent data is read into the RAM. If an attempt is made to read this data it is accessed from RAM rather than from the disk, thus considerably reducing access times.

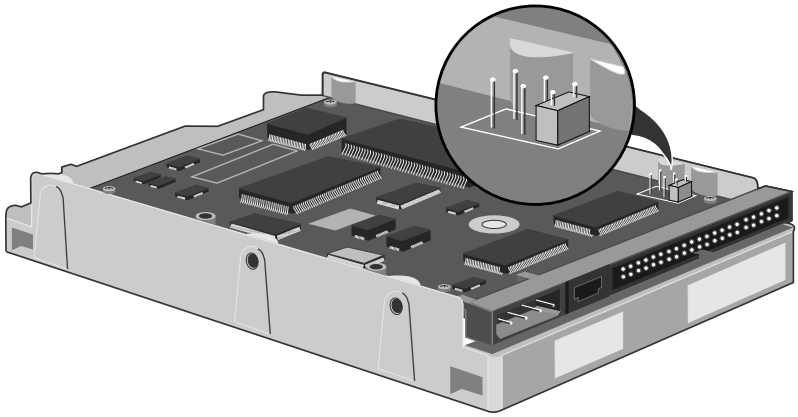
Quantum ProDrive LPS 240AT

The 240 Mbyte hard disk drive that may be fitted in the LS Pro range is a Quantum ProDrive LPS 240AT. It has a nominal access time of 16mS and can transfer data at up to 5.0 Mbytes per second.

The drive circuit board contains the drive control electronics and a hard disk controller. A preamplifier for the read/write circuitry and an optical encoder are located underneath the drive cover.

The drives feature an on-board media defect and error recovery scheme which is fully user transparent.

Jumpers Four jumpers on the drive circuit are used to configure the drive. These are shown, properly configured, in the following illustration.



The jumpers are labelled CS (Cable select), DS (Drive select), SP (Slave present) and DM (Drive Mode). The DS jumper must be fitted and the CS, SP and DM jumpers not, in order for the drive to function in an LS Pro.

Drive format The physical format of the drive is as follows:

Disks	2
Heads	4
Tracks	7,200

Formatting

These drives are low level formatted during manufacture. This format has been optimized to allow the drive to provide maximum performance. Standard low level formatting programs can only reduce the performance of the drive.

Warning

Do not attempt to perform a low level format on a ProDrive, this can only adversely affect the performance of your drive. If you do try to format your drive most standard low level formatting programs will return a "Drive formatted" message very quickly. In fact, the drive has not been formatted.

Discache

The ProDrive LPS 240AT drive is fitted with 256kbytes of RAM and look-ahead cache circuitry known as Discache.

When a read access is made to the drive, Discache loads subsequent data into the RAM. If an attempt is made to read this data it is accessed from RAM rather than from the disk, thus considerably reducing access times.

Cache performance benefits tend to be application dependent. Discache has a number of alterable parameters which allow the cache to be configured for maximum performance benefit in any given application.

Full information on configuring Discache is given in the Quantum specification.

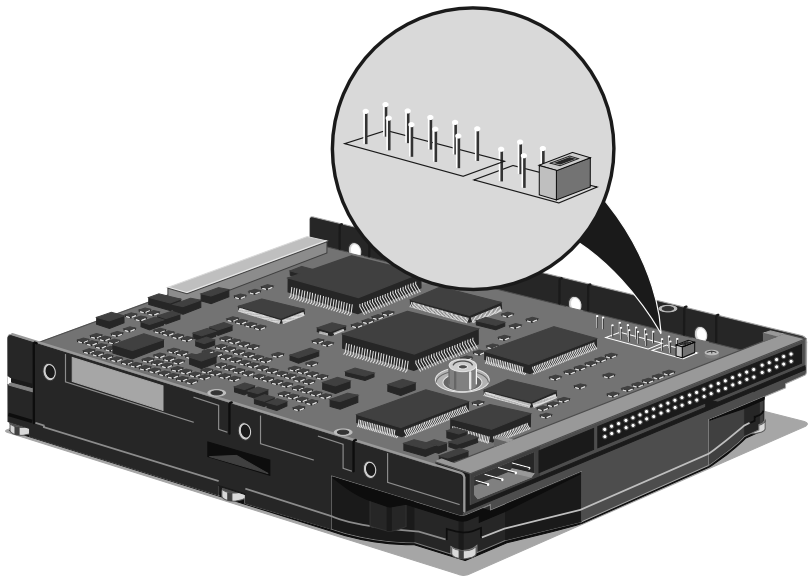
Quantum LPS525A

The 525 Mbyte hard disk drive that may be fitted in the LS Pro range is a Quantum LPS525A. It has a nominal access time of 10mS and can transfer data at up to 5 Mbytes per second.

The drive circuit board contains the drive control electronics and a hard disk controller. The drive features an on-board media defect and error recovery scheme which is fully user transparent.

Jumpers

Three jumpers on the drive circuit are used to configure the drive. These are shown in the following illustration.



The three jumpers are labelled DS (Drive select), CS (Cable select) and SP (Slave present). In the LS Pro application the DS jumper must be fitted and the CS and SS jumpers not.

Warning

None of the other jumpers are used in this application. If any of the other jumpers are installed the drive will not function correctly.

Drive format

The physical format of the drive is as follows:

Disks	3
Heads	6
Tracks	14,688

Formatting

The drive is low level formatted during manufacture. This format has been optimized to allow the drive to provide maximum performance. Standard low level formatting programs can only reduce the performance of the drive.

Warning

Do not attempt to perform a low level format on a ProDrive, this can only adversely affect the performance of your drive. If you do try to format your drive most standard low level formatting programs will return a "Drive formatted" message very quickly. In fact, the drive has not been formatted.

Discache

The ProDrive LPS 525AT drive is fitted with 512kbytes of RAM and look-ahead cache circuitry known as Discache.

When a read access is made to the drive, Discache loads subsequent data into the RAM. If an attempt is made to read this data it is accessed from RAM rather than from the disk, thus considerably reducing access times.

Cache performance benefits tend to be application dependent. Discache has a number of alterable parameters which allow the cache to be configured for maximum performance benefit in any given application.

Full information on configuring Discache is given in the Quantum specification.

IDE interface

Interface signal descriptions

Host reset

Reset signal from the system board. Active low during system power up.

Host data 0-15

16-bit bidirectional data bus between the system board and the drive.

Host I/O channel ready

These two lines allow the drive to lengthen I/O read and write cycles by generating system board wait states. These lines are normally high and are driven low by the drive if an I/O cycle is to be lengthened.

Host IOW

Write strobe. This signal clocks data from the system board to the drive on the data bus.

Host IOR

Read strobe. This signal clocks data from the drive to the system board on the data bus.

Host ALE

System board Address Latch Enable. This signal is not used by the drive, it is provided for compatibility.

Host IRQ14

This is the interrupt signal to the system board. This signal is active high when the drive is selected and the drive interrupt enable bit (IEN) is activated by the system board. An interrupt is cleared upon receiving the next command, when the status register is read, or when the drive is reset.

Host IOCS16

Informs the system board that the drive data register has been enabled and the drive is prepared to perform a 16-bit I/O transfer.

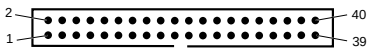
Host ADDR 0-2

These lines are used to select registers on the drive.

Connectors *Control Connector*

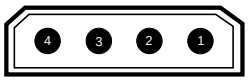
Pin	Function	Pin	Function
1	host reset-	21	host I/O channel ready-
2	ground	22	ground
3	host data 7	23	host IOW-
4	host data 8	24	ground
5	host data 6	25	host IOR-
6	host data 9	26	ground
7	host data 5	27	host I/O channel ready-
8	host data 10	28	host ALE
9	host data 4	29	reserved
10	host data 11	30	ground
11	host data 3	31	host IRQ14
12	host data 12	32	host IOCS16-
13	host data 2	33	host ADDR1
14	host data 13	34	-
15	host data 1	35	host ADDR0
16	host data 14	36	host ADDR2
17	host data 0	37	-
18	host data 15	38	-
19	ground	39	-
20	key	40	ground

The pin layout of the connector.



Power connector

Pin	Function
1	+12 Volts
2	ground (for +12V)
3	ground (for +5V)
4	+5 Volts



4.4 FLOPPY DRIVE

Description

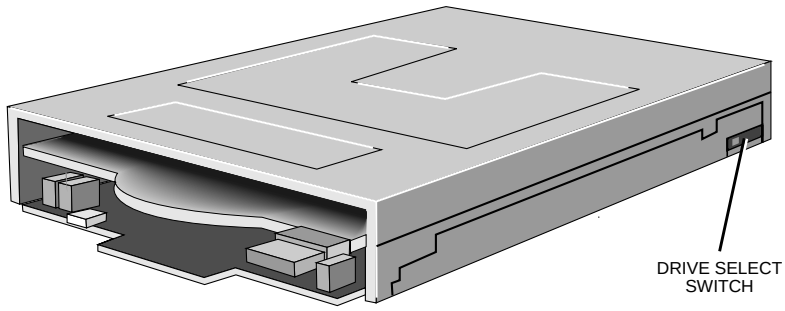
The floppy disk drive fitted in the LS Pro range is a 3.5", high density double-sided, one inch high unit. The drive can read and write 3.5" discs with a formatted capacity of either 1.44Mbytes or 720 kbytes. The drive has a constant disk rotation speed of 300 rpm. The different disk capacities are accommodated by different data transfer rates.

The 1.44 Mbyte media uses a data transfer rate of 500 kbits/sec. The 720 kbyte media uses a data transfer rate of 250 kbits/sec.

Both types of media are double-sided with 80 tracks per side and a track density of 135 tracks per inch.

Drive select switch

The drive select switch is set to identify the drive to the system. The switch is located at the rear of the drive on the right-hand side. The switch is set to 0. The drive select switch is shown below.



Disk format

1.44 Mbyte disks have a hole in the disk in the opposite corner to the write protect tab. The drive uses this to determine the type of disk fitted. If the drive does not detect a hole in the disk it treats it as a 720kbyte disk and changes the transfer rate to 250 kbits per second.

The following details briefly describe the floppy disk formats for the two capacities of disk.

720 kbytes disks

- double-sided
- 80 tracks/side
- 512 bytes/sector
- 9 sectors/track

1.44 Mbyte disks

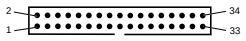
- double-sided
- 80 tracks/side
- 512 bytes/sector
- 18 sectors/track

Interface

The drive has one connector. The pinout of the connector and an illustration are shown below.

Connector

Pin	Function	Pin	Function
2	density select 1	14	drive select 2
3	not connected	16	motor on
4	not connected	18	direction
5	5V	20	step
6	density select 0	22	write data
7	5V	24	write enable
8	index	26	track 00
9	5V	28	write protect
10	drive select 0	30	read data
11	5V	32	head select
12	drive select 1	34	disk change



Note

All other pins are connected to 0 Volts.

Signal descriptions

Density select 0,1

Not currently used.

Drive select 0,1,2

The drive select inputs are used to enable and disable the other input/output lines. When a select input is low the drive is active and the input/output lines are enabled. When a select input is high, all outputs from the drive are disabled and all inputs are ignored.

Index

When the drive is selected this line is pulsed low for each revolution of the disk drive spindle.

Motor on

When this input is taken low and a disk is inserted in the drive, the drive motor starts. When this input is taken high or a disk is removed the drive motor stops.

Direction

If this input is high the step input causes the read/write head to step away from the centre of the disk. If this input is low the head steps toward the centre of the disk.

Step

A low pulse on this input will cause the read/write head to move to the next track. The direction of movement is determined by the direction input at the end of the step pulse.

Write data

If the write gate input is low, a low pulse on this input will write a bit of data on the disk.

Write gate

If this input is low, the write circuitry is enabled and data can be written to the disk via the write data input.

Track 00

This is an output which is low when the read/write head is positioned on track 00 of the disk.

Write protect

If a write protected disk is in the drive this output is low and the drive is unable to write data.

Read data

When the drive is selected a low pulse is generated for each bit on the disk that is detected.

Head select

This input selects the read/write head. If low, head 1 is selected, if high, head 0 is selected.

Disk change

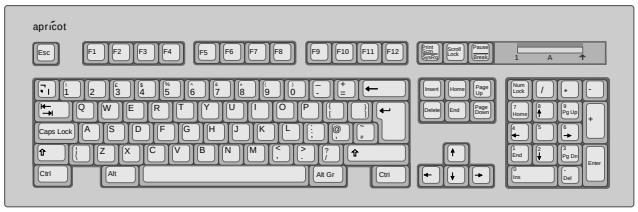
This output is low whenever a disk is removed from the drive. It remains low until a disk is inserted, and the disk change reset signal has been received.

4.5 KEYBOARD

Introduction

The keyboard has 102-keys in the same layout as the IBM AT enhanced keyboard. It provides the full range of QWERTY typewriter keys, special editing and function keys and a number pad at the right hand side of the keyboard.

The following illustration shows the layout of the keys and the key legends on the UK keyboard.



Operation

The keyboard communicates with the keyboard interface in the system unit using two lines: clock and data. These lines are driven by both the keyboard and the system unit. The keyboard provides the clock for both transmitting and receiving.

Communication is bi-directional. The system unit can send commands to the keyboard as well as the keyboard sending scan codes to the system unit. The keyboard first checks the clock line: if it is low, pending scan codes are loaded into the keyboard buffer; if the clock line is high the keyboard checks the data line.

If the data line is low the keyboard receives commands from the system unit, if the data line is high the keyboard sends data to the system unit. The data consists of: one start bit; eight data bits; and one parity bit. Each time the keyboard takes the clock line high it checks to see if the system unit is pulling the line low. If the line has been pulled low the code being transmitted is saved and the keyboard enters the receive mode.

Commands to the system unit

The keyboard sends data and command codes to the system unit. The commands that the keyboard can send are described in the following table.

Command	Function
FEh	resend
FCh	self-test failure
FAh	acknowledge
EEh	echo response
AAh	self-test pass
00h or FFh	buffer overflow
83ABh	identification byte

Resend (FEh)

The keyboard sends this command to the system unit if it receives an invalid command, or a command with bad parity.

Self-test failure (FCh)

If the keyboard RAM or ROM self-test fails, this command is sent.

Acknowledge (FAh)

The keyboard sends this command after receiving a valid input from the system unit. There are two exceptions: in response to an echo command; and usually in response to a resend command. However, a resend command will result in an acknowledge response if acknowledge was the last transmission to the keyboard.

Echo (EEh)

This is sent in response to an echo command from the system unit.

Self-test pass (AAh)

This code is sent to the system unit if the keyboard RAM and ROM self-test is passed.

Buffer overflow (00h or FFh)

This code is sent to the system unit when the type ahead buffer overflows. 00h is sent if code sets 2 or 3 are in use; FFh is sent if code set 1 is in use.

Identification byte (83ABh)

These bytes are sent to the system unit in response to a read ID command. The keyboard stops scanning, sends the ID bytes, then continues scanning. The least significant byte is sent first.

Commands from the system unit

Commands are sent from the system unit to the keyboard via the keyboard controller data buffer. The controller inserts a parity bit and transmits the data serially to the keyboard. No further transmission is sent to the keyboard until the keyboard acknowledges receipt of the data byte.

The command bytes which the keyboard recognises are listed below.

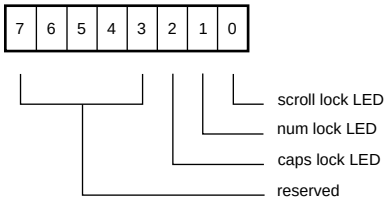
Command	Description
EDh	Set/reset LED indicators
EEh	Echo
EFh	No operation
F0h	Select alternate scan codes
F1h	No operation
F2h	Read ID
F3h	Set typematic rate/delay
F4h	Enable
F5h	Default disable
F6h	Set default
F7h	Set all keys typematic
F8h	Set all keys make/break
F9h	Set all keys make only
FAh	Set all keys typematic/make/break
FBh	Set key to typematic
FCh	Set key to make/break
FEh	Resend
FFh	Reset

When the keyboard receives any of these commands, it sends an ACKnowledge (FAh) response. If the data is incorrectly received the keyboard sends a RESEND (FEh) request.

The use and formats of these commands is described in the following paragraphs.

Set/reset LED indicators (EDh)

This command is used to set the LEDs on the keyboard. When the keyboard receives this command it responds with the ACK (FAh). The controller then sends the parameter byte. On receipt of the parameter byte the keyboard updates the LEDs. The format of the parameter byte is shown below:



Note

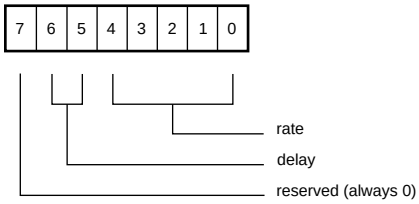
Bit 7 must be set to 0.

Echo (EEh)

The keyboard responds to this command by sending an "echo response" (EEh), and then continues with normal operation.

Set typematic rate/delay (F3h)

The keyboard responds with an ACK, stops scanning, and waits for the rate/delay byte from the system unit. The format of the byte is as follows.



Rate Parameter

The typematic rate (number of make codes per second) is from 2 make codes per second with bits D0 to D4 all set to 1, to 30 make codes per second, with bits D0 to D4 all set to 0.

Delay Parameter

The delay before the typematic operation comes into effect is shown in the table below:

D6	D5	Delay
0	0	250mS
0	1	500mS
1	0	750mS
1	1	1000mS

Enable (F4h)

The keyboard responds with an ACK, clears its output buffer, and enables key scanning and keycode transmission.

Default disable (F5h)

The keyboard performs the same functions as "Set default" except that further scanning and transmission is disabled.

Set default (F6h)

The keyboard resets, clears its buffers, and responds with an ACK. If it was previously enabled it then resumes normal scanning/transmission.

Set all keys (F7h, F8h, F9h and FAh)

These commands are only valid when the keyboard is set to "code set three". The different code sets are described elsewhere in this section. The commands set all of the keys to be the type specified: typematic (F7h), make/break (F8h), make only (F9h) and typematic/make/break (FAh).

Set key type (FBh, FCh and FDh)

These commands are only valid when the keyboard is set to "code set three". The different code sets are described elsewhere in this section. The commands set individual keys to be the type specified: typematic (FBh), make/break (FCh) and make only (FDh). The command is first sent, the keyboard acknowledges the command and waits for the key scan code to be sent. One or more key codes can be sent. The keyboard then waits for an ENABLE (F4h) before resuming scanning.

Resend (FEh)

The keyboard resends the last code sent to the system unit.

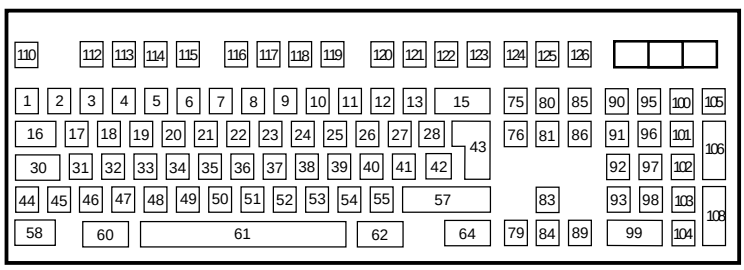
Reset (FFh)

The keyboard responds with an ACK, performs a set of internal diagnostics, clears its key buffer, and then sets the typematic rate/delay to the default values.

Scan codes

Three sets of scan codes are available. The keyboard normally selects code set 2 (AT compatible). The other sets may be selected using select alternative scan codes command (F0h).

The following diagram numbers the positions which are referred to in the following scan code tables.



Scan code set 1

These scan codes are compatible with the PC/XT keyboard scan codes. Each key is assigned a make code which is sent to the keyboard buffer when the key is pressed. The break code is sent when the key is released. The break codes are generated by adding 80h to the make codes. Notice that some of the scan codes have additional codes. These are for additional keys and to indicate shift states.

The codes are listed in the following table:

Scan code set 1

Key Number	Make Code	Break Code
1	29	A9
2	02	82
3	03	83
4	04	84
5	05	85
6	06	86
7	07	87
8	08	88
9	09	89
10	0A	8A
11	0B	8B
12	0C	8C
13	0D	8D
15	0E	8E
16	0F	8F
17	10	90
18	11	91
19	12	92
20	13	93
21	14	94
22	15	95
23	16	96
24	17	97
25	18	98
26	19	99
27	1A	9A
28	1B	9B
30	3A	BA
31	1E	9E
32	1F	9F
33	20	A0
34	21	A1
35	22	A2
36	23	A3
37	24	A4
38	25	A5
39	26	A6
40	27	A7
41	28	A8
42	2B	AB
43	1C	9C

Key Number	Make Code	Break Code
44	2A	AA
45	56	D6
46	2C	AC
47	2D	AD
48	2E	AE
49	2F	AF
50	30	B0
51	31	B1
52	32	B2
53	33	B3
54	34	B4
55	35	B5
57	36	B6
58	1D	9D
60	38	B8
61	39	B9
62	E0 38	E0 B8
64	E0 1D	E0 9D
90	45	C5
91	47	C7
92	4B	CB
93	4F	CF
95	E0 35	E0 B5
96	48	C8
97	4C	CC
98	50	D0
99	52	D2
100	37	B7
101	49	C9
102	4D	CD
103	51	D1
104	53	D3
105	4A	CA
106	4E	CE
108	E0 1C	E0 9C
110	01	81
112	3B	BB
113	3C	BC
114	3D	BD
115	3E	BE
116	3F	BF

Key Number	Make Code	Break Code
117	40	C0
118	41	C1
119	42	C2
120	43	C3
121	44	C4
122	57	D7
123	58	D8
124	E0 2A	E0 B7
	E0 37	E0 AA
125	46	C6
126	E1 D1 45	This key
	E1 9D C5	does not
		have a
		break code
Lower-case or Shift and Num Lock keys active		
75	E0 52	E0 D2
76	E0 53	E0 D3
79	E0 4B	E0 CB
80	E0 47	E0 C7
81	E0 4F	E0 CF
83	E0 48	E0 C8
84	E0 50	E0 D0
85	E0 49	E0 C9
86	E0 51	E0 D1
89	E0 4D	E0 CD
Shift key active		
75	E0 AA E0 52	E0 D2 E0 2A
76	E0 AA E0 53	E0 D3 E0 2A
79	E0 AA E0 4B	E0 CB E0 2A
80	E0 AA E0 47	E0 C7 E0 2A
81	E0 AA E0 4F	E0 CF E0 2A
83	E0 AA E0 48	E0 C8 E0 2A
84	E0 AA E0 50	E0 D0 D0 2A
85	E0 AA E0 49	E0 C9 E0 2A
86	E0 AA E0 51	E0 D1 E0 2A
89	E0 AA E0 4D	E0 CD E0 2A
95	E0 AA E0 35	E0 B5 E0 2A

Key Number	Make Code	Break Code
Num Lock key active		
75	E0 2A E0 52	E0 D2 E0 AA
76	E0 2A E0 53	E0 D3 E0 AA
79	E0 2A E0 4B	E0 CB E0 AA
80	E0 2A E0 47	E0 C7 E0 AA
81	E0 2A E0 4F	E0 CF E0 AA
83	E0 2A E0 48	E0 C8 E0 AA
84	E0 2A E0 50	E0 D0 E0 AA
85	E0 2A E0 49	E0 C9 E0 AA
86	E0 2A E0 51	E0 D1 E0 AA
89	E0 2A E0 4D	E0 CD E0 AA
Ctrl or Shift keys active		
124	E0 37	E0 B7
Alt key active		
124	54	D4
Ctrl key active		
126	E0 46 E0 C6	This key
		does not
		have a
		break code

Scan code set 2 These scan codes are AT/PS/2 compatible. Each key is assigned a make code which is sent to the keyboard buffer when the key is pressed. The break code is sent when the key is released. The break codes are produced by sending F0h followed by the make code. Notice that some of the scan codes have additional codes to indicate the various shift states.

Scan Code set 2

Key Number	Make Code	Break Code
1	0E	F0 0E
2	16	F0 16
3	1E	F0 1E
4	26	F0 26
5	25	F0 25
6	2E	F0 2E
7	36	F0 36
8	3D	F0 3D
9	3E	F0 3E
10	46	F0 46
11	45	F0 45
12	4E	F0 4E
13	55	F0 55
15	66	F0 66
16	0D	F0 0D
17	15	F0 15
18	1D	F0 1D
19	24	F0 24
20	2D	F0 2D
21	2C	F0 2C
22	35	F0 35
23	3C	F0 3C
24	43	F0 43
25	44	F0 44
26	4D	F0 4D
27	54	F0 54
28	5B	F0 5B
30	58	F0 58
31	1C	F0 1C
32	1B	F0 1B
33	23	F0 23
34	2B	F0 2B
35	34	F0 34
36	33	F0 33
37	3B	F0 3B
38	42	F0 42
39	4B	F0 4B
40	4C	F0 4C
41	52	F0 52
42	5D	F0 5D

Key Number	Make Code	Break Code
43	5A	F0 5A
44	12	F0 12
45	61	F0 61
46	1A	F0 1A
47	22	F0 22
48	21	F0 21
49	2A	F0 2A
50	32	F0 32
51	31	F0 32
52	3A	F0 3A
53	41	F0 41
54	49	F0 49
55	4A	F0 4A
57	59	F0 59
58	14	F0 14
60	11	F0 11
61	29	F0 29
62	E0 11	E0 F0 11
64	E0 14	E0 F0 14
90	77	F0 77
91	6C	F0 6C
92	68	F0 68
93	69	F0 69
95	E0 4A	E0 F0 4A
96	75	F0 75
97	73	F0 73
98	72	F0 72
99	70	F0 70
100	7C	F0 7C
101	7D	F0 7D
102	74	F0 74
103	7A	F0 7A
104	71	F0 71
105	7B	F0 7B
106	79	F0 79
108	E0 5A	E0 F0 5A
110	76	F0 76
112	05	F0 05
113	06	F0 06
114	04	F0 04

Key Number	Make Code	Break Code
115	0C	F0 0C
116	03	F0 03
117	0B	F0 0B
118	83	F0 83
119	0A	F0 0A
120	01	F0 01
121	09	F0 09
122	78	F0 78
123	07	F0 07
124	E0 12 E0 7C	E0 F0 7C E0 F0 12
125	7E	F0 7E
126	E1 14 77 E1 F0 14 F0 77	This key does not have a break code
Lower-case or Shift and Num Lock keys active		
75	E0 70	E0 F0 70
76	E0 71	E0 F0 71
79	E0 6B	E0 F0 6B
80	E0 6C	E0 F0 6C
81	E0 69	E0 F0 69
83	E0 75	E0 F0 75
84	E0 72	E0 F0 72
85	E0 7D	E0 F0 7D
86	E0 7A	E0 F0 7A
89	E0 74	E0 F0 74

Key Number	Make Code	Break Code
Shift key active		
75	E0 F0 12 E0 70	E0 F0 70 E0 12
76	E0 F0 12 E0 71	E0 F0 71 E0 12
79	E0 F0 12 E0 6B	E0 F0 6B E0 12
80	E0 F0 12 E0 6C	E0 F0 6C E0 12
81	E0 F0 12 E0 69	E0 F0 69 E0 12
83	E0 F0 12 E0 75	E0 F0 75 E0 12
84	E0 F0 12 E0 7D	E0 F0 7D E0 12
85	E0 F0 12 E0 7A	E0 F0 7A E0 12
86	E0 F0 12 E0 74	E0 F0 74 E0 12
89	E0 F0 12 E0 74	E0 F0 74 E0 12
95	E0 F0 12 4A	E0 12 F0 4A
Num Lock key active		
75	E0 12 E0 70	E0 F0 70 E0 F0 12
76	E0 12 E0 71	E0 F0 71 E0 F0 12
79	E0 12 E0 6B	E0 F0 6B E0 F0 12
80	E0 12 E0 6C	E0 F0 6C E0 F0 12
81	E0 12 E0 69	E0 F0 69 E0 F0 12
83	E0 12 E0 75	E0 F0 75 E0 F0 12
84	E0 12 E0 72	E0 F0 72 E0 F0 12
85	E0 12 E0 7D	E0 F0 7D E0 F0 12
86	E0 12 E0 7A	E0 F0 7A E0 F0 12
89	E0 12 E0 74	E0 F0 74 E0 F0 12
Ctrl or Shift keys active		
124	E0 7C	E0 F0 7C
Alt key active		
124	84	F0 84
Ctrl key active		
126	E0 7E E0 F0 7E	This key does not have a break code

Scan set 3 Each key is assigned a make code which is sent to the keyboard buffer when the key is pressed. The break code is sent when the key is released. The break codes are produced by sending F0h followed by the make code. The codes are not affected by any shift states within the keyboard. The keys are defined as typematic, make/break or make only. The type of key can be changed by using the set all keys command (F7, F8, F9, FA) to the keyboard from the system unit.

Scan Code set 3

Key Number	Make Code	Break Code	Key type
1	0E	F0 0E	Typematic
2	16	F0 16	Typematic
3	1E	F0 1E	Typematic
4	26	F0 26	Typematic
5	25	F0 25	Typematic
6	2E	F0 2E	Typematic
7	36	F0 36	Typematic
8	3D	F0 3D	Typematic
9	3E	F0 3E	Typematic
10	46	F0 46	Typematic
11	45	F0 45	Typematic
12	4E	F0 4E	Typematic
13	55	F0 55	Typematic
15	66	F0 66	Typematic
16	0D	F0 0D	Typematic
17	15	F0 15	Typematic
18	1D	F0 1D	Typematic
19	24	F0 24	Typematic
20	2D	F0 2D	Typematic
21	2C	F0 2C	Typematic
22	35	F0 35	Typematic
23	3C	F0 3C	Typematic
24	43	F0 43	Typematic
25	44	F0 44	Typematic
26	4D	F0 4D	Typematic
27	54	F0 54	Typematic
28	5B	F0 5B	Typematic
30	14	F0 14	Make/break
31	1C	F0 1C	Typematic
32	1B	F0 1B	Typematic
33	23	F0 23	Typematic
34	2B	F0 2B	Typematic
35	34	F0 34	Typematic
36	33	F0 33	Typematic
37	3B	F0 3B	Typematic
38	42	F0 42	Typematic
39	4B	F0 4B	Typematic
40	4C	F0 4C	Typematic

Key Number	Make Code	Break Code	Key type
41	52	F0 52	Typematic
42	53	F0 53	Typematic
43	5A	F0 5A	Typematic
44	12	F0 12	Make/break
45	13	F0 13	Typematic
46	1A	F0 1A	Typematic
47	22	F0 22	Typematic
48	21	F0 21	Typematic
49	2A	F0 2A	Typematic
50	32	F0 32	Typematic
51	31	F0 31	Typematic
52	3A	F0 3A	Typematic
53	41	F0 41	Typematic
54	49	F0 49	Typematic
55	4A	F0 4A	Typematic
57	59	F0 59	Make/break
58	11	F0 11	Make/break
60	19	F0 19	Make/break
61	29	F0 29	Typematic
62	39	F0 39	Make only
64	58	F0 58	Make only
75	67	F0 67	Make only
76	64	F0 64	Typematic
79	61	F0 61	Typematic
80	6E	F0 6E	Make only
81	65	FO 65	Make only
83	63	F0 63	Typematic
84	60	F0 60	Typematic
85	6F	F0 6F	Make only
86	6D	F0 6D	Make only
89	6A	F0 6A	Typematic
90	76	F0 76	Make only
91	6C	F0 6C	Make only
92	6B	F0 6B	Make only
93	69	F0 69	Make only
95	77	F0 77	Make only
96	75	F0 75	Make only
97	73	F0 73	Make only

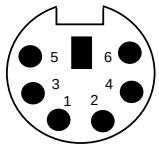
Key Number	Make Code	Break Code	Key type
98	72	F0 72	Make only
100	7E	F0 7E	Make only
101	7D	F0 7D	Make only
102	74	F0 74	Make only
103	7A	F0 7A	Make only
104	71	F0 71	Make only
105	84	F0 84	Make only
106	7C	F0 7C	Typematic
108	79	F0 79	Make only
110	08	F0 08	Make only
112	07	F0 07	Make only
113	0F	F0 0F	Make only
114	17	F0 17	Make only

Key Number	Make Code	Break Code	Key type
115	1F	F0 1F	Make only
116	27	F0 27	Make only
117	2F	F0 2F	Make only
118	37	F0 37	Make only
119	3F	F0 3F	Make only
120	47	F0 47	Make only
121	4F	F0 4F	Make only
122	56	F0 56	Make only
123	5E	F0 5E	Make only
124	57	F0 57	Make only
125	5F	F0 5F	Make only
126	62	F0 62	Make only

Connector

The keyboard is connected to the system unit via a 6-pin miniature DIN connector. The pinout and connector details are given below.

Pin	I/O	Signal name
1	I/O	Data
2	NA	Reserved
3	NA	Ground
4	NA	+5Vdc
5	I/O	Clock
6	NA	Reserved



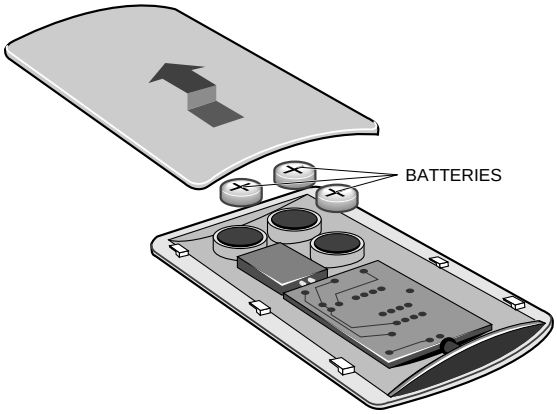
4.6 KeyLOC CARD

The KeyLOC card is a credit card sized unit which is used in conjunction with the Apricot LOC Technology software to control access to the computer and the data stored on it.

The KeyLOC card consists of a plastic case and a small circuit board. The plastic case is in two halves and contains the circuit board and three small batteries. The case may be opened in order to replace the batteries, this is done by sliding the two halves apart. The batteries should be replaced with Duracell 389 or equivalent and should be placed in the holder positive pole upwards.

Note

Take care not to touch the surfaces of the batteries during installation.



The circuit board contains a small 4-bit microprocessor system, a switch and an infra red transmitter. Each time the switch is operated the microprocessor generates a pseudo-random bit pattern which is transmitted by the infra red transmitter. This signal is received by the infra red detector on the LED card within the system unit and passed to the security sub-system on the system board.

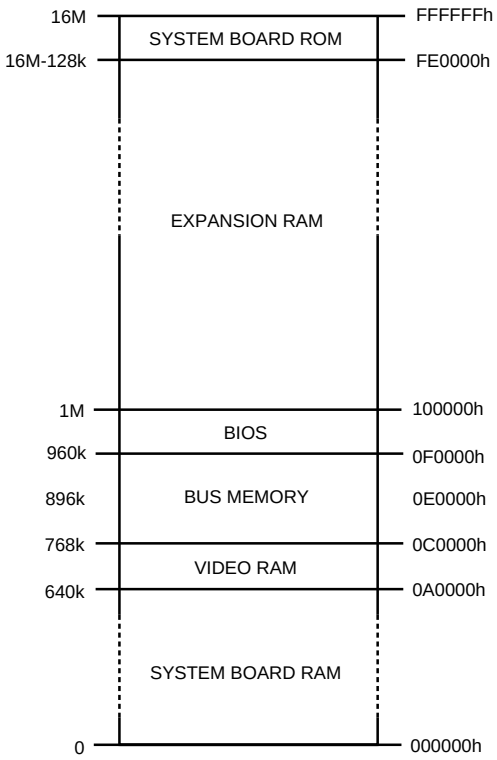
Contents

5.1 INTRODUCTION

This section describes Memory and I/O space layout, and details the usage of the registers in I/O space.

5.2 MEMORY USAGE

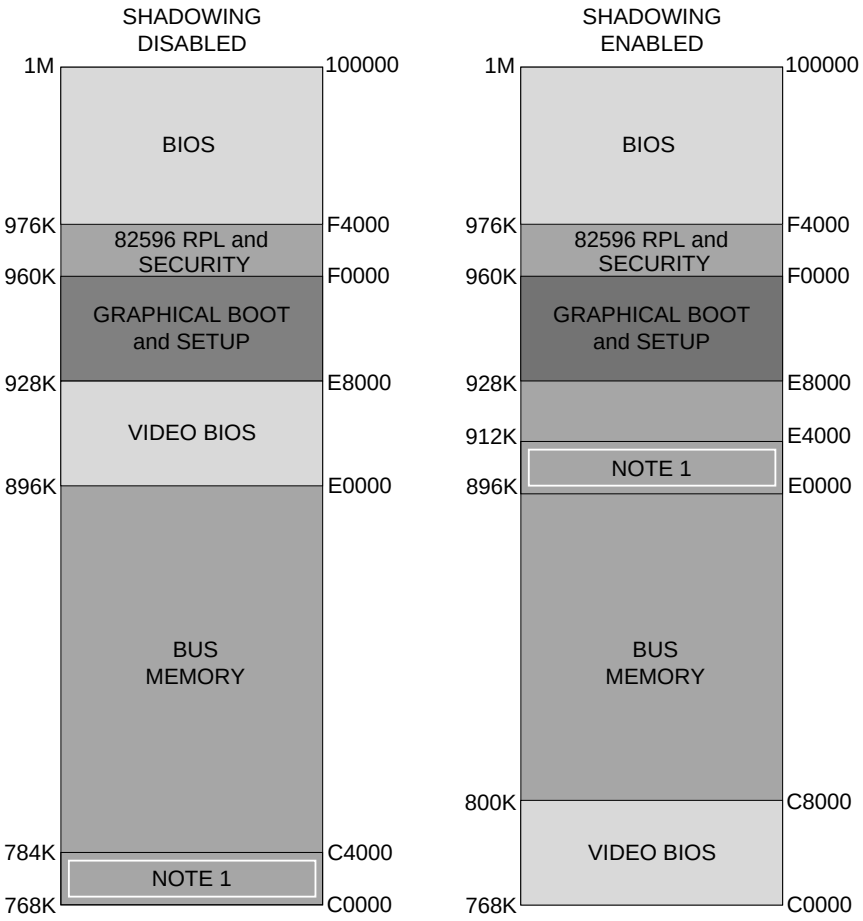
The memory map below details the addressing of system board memory.



Note

The SETUP utility allows BIOS shadowing to be enabled or disabled. If shadowing is enabled the BIOS on the system board is copied into RAM where it can be accessed faster.

A more detailed description of the region between 768k and 1M (0C0000h and 100000h) is given over.



Notes

1. *This area is occupied by the ROM in the option ROM socket if it is fitted.*
2. *These memory maps do not include the Token-Ring module RAM and ROM. If fitted the ROM occupies an 16k block between CC000h and D0000h. The RAM buffer size and base address are configured by the adapter driver.*

The video BIOS, graphical boot and SETUP, 82596 RPL and security and system BIOS code are all in the main 128kbyte system ROM. After boot is completed only the video BIOS and system BIOS code is required.

Shadowing disabled

With shadowing disabled and the option ROM socket empty the regions from C0000 to E0000 and from E8000 to F4000 are available as UMB space for DOS.

Shadowing enabled

When shadowing is enabled the video BIOS is remapped to the C0000 to C8000 area. Thus with the shadowing enabled and the option ROM socket empty the region from C8000 to F4000 is available as UMB space for DOS. This is the same amount of UMB as is available with shadowing disabled, but it is contiguous. This often allows DOS to make better use of the available space.

Note

The Rev C system board has a slightly different memory map, refer to Appendix B for details.

5.3 I/O SPACE

The table below shows the general use of I/O space on the LS Pro system board. The pages which follow describe in more detail specific ports and groups of ports.

Addresses (hex)	Device
0000-000F	Master DMA controller
0020-0021	Master interrupt controller
0040-0043	System timers
0060	Keyboard controller
0061	Port B (PPI control port)
0064	Keyboard controller
0070-0071	RTC RAM/NMI mask
0080-008F	DMA page registers
00A0-00A1	Slave interrupt controller
00C0-00DF	Slave DMA controller
00E8-00FE	SCAMP
0120-012F	Apricot ports
01F0-01F7	Hard disk drive
02F8-02FF	Serial port 2
0300-030F	Ethernet controller
0388-038F	Business audio
03B4, 03B5, 03BA	VGA
03BC-03BE	Parallel port controller
03C0-03C5	VGA
03C6-03C9	Video DAC
03CE, 03CF, 03D4	VGA
03D5, 03DA	VGA
03F2-03F5	Floppy disk controller
03F6, 03F7	Floppy and hard disk controller
03F8-03FF	Serial port 1
46E8	VGA setup

DMA I/O address map

The following table shows the I/O addresses used by the DMA Controller and their significance. Full information on the programming of 8237 DMA controller registers are given in manufacturers data sheets and are not repeated here

Address (hex)	Function
0000	Channel 0 Memory address register
0001	Channel 0 Transfer count register
0002	Channel 1 Memory address register
0003	Channel 1 Transfer count register
0004	Channel 2 Memory address register
0005	Channel 2 Transfer count register
0006	Channel 3 Memory address register
0007	Channel 3 Transfer count register
0008	Channel 0-3 Status register
0009	Reserved
000A	Channel 0-3 Mask Register (set/reset)
000B	Channel 0-3 Mode register (write)
000C	Clear byte pointer (write)
000D	Master clear (write)
000E	Channel 0-3 Clear mask register (write)
000F	Channel 0-3 Write mask register
0080	Diagnostic checkpoint port
0081	Channel 2 Page table address register
0082	Channel 3 Page table address register
0083	Channel 1 Page table address register
0087	Channel 0 Page table address register
0089	Channel 6 Page table address register
008A	Channel 7 Page table address register
008B	Channel 5 Page table address register
008F	Channel 4 Page table address register
00C0	Channel 4 Memory address register
00C2	Channel 4 Transfer count register
00C4	Channel 5 Memory address register
00C6	Channel 5 Transfer count register
00C8	Channel 6 Memory address register
00CA	Channel 6 Transfer count register
00CC	Channel 7 Memory address register
00CE	Channel 7 Transfer count register
00D0	Channel 4-7 Status register
00D4	Channel 4-7 Mask register (set/reset)
00D6	Channel 4-7 Mode register (write)
00D8	Clear byte pointer (write)
00DA	Master clear (write)
00DC	Channel 4-7 Clear mask register (write)
00DE	Channel 4-7 Write mask register

Interrupt controllers

The interrupt controllers are programmed by writing to four 8-bit I/O ports. These are listed in the following table.

Address	R/W	Function
Master controller		
0020h	R/W	Port 1
0021h	R/W	Port 2
Slave controller		
00A0h	R/W	Port 1
00A1h	R/W	Port 2

Full details on programming 8259 interrupt controllers are given in the manufacturers data sheet.

System timers

The 8254 compatible system timer is accessed at I/O locations 0040h-0043h. The following table identifies the function of each port.

Address	Function
0040h	Counter 0 count
0041h	Counter 1 count
0042h	Counter 2 count
0043h	Control register

A full description of programming 8254 timers is included in the manufacturers specification and is not repeated here.

Keyboard controller

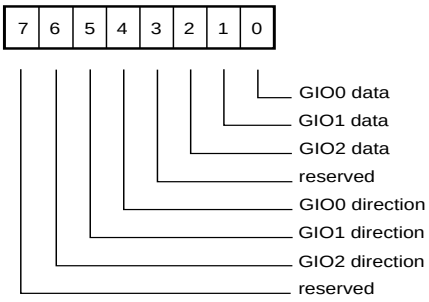
The 8042 keyboard controller has two ports which are in I/O space at locations 0060h and 0064h. The port at 0060h is an output port where keyboard data is made available to the system. The port at 0064h is the command/status port which is described in more detail below.

Command/status port

When the system reads I/O location 0064h it receives information about the status of the controller. When the system writes to I/O location 0064h the byte is interpreted as a command.

Write

A write to port 0064h has the following significance.



Bit 0 When this bit is set to 1 the keyboard controller generates an interrupt when keyboard data is placed in it's output buffer.

Bit 1 Reserved.

Bit 2 The system flag bit in the keyboard controller status register reflects the state of this bit.

Bit 3 Reserved.

Bit 4 When this bit is set to 1 the keyboard interface is disabled.

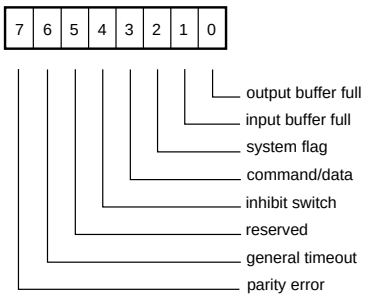
Bit 5 Reserved.

Bit 6 When this bit is set to 1 the incoming scan codes are translated to scan code set 1 listed in section 4. When this bit is set to 0 the incoming scan codes are passed on unaffected.

Bit 7 Reserved.

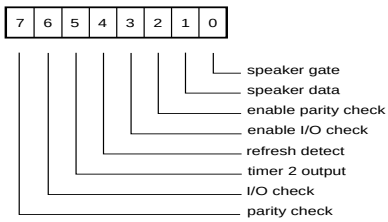
Read

A read from port 0064h has the following significance.



Port B

Write operations



Bit 0 Setting this bit to 1 enables the timer 2 gate. Setting this bit to 0 disables the timer 2 gate.

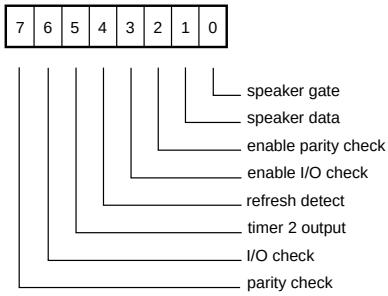
Bit 1 Setting this bit to 1 enables speaker data. This bit is set to 0 during a system reset.

Bit 2 Setting this bit to 0 enables Parity check. This bit is set to 1 during a system reset.

Bit 3 Setting this bit to 0 enables an I/O check. This bit is set to 1 during a system reset.

Bits 4-7 Reserved

Read operations



Bit 0 A read operation returns the result of the last write operation to this bit.

Bit 1 A read operation returns the result of the last write operation to this bit.

Bit 2 A read operation returns the result of the last write operation to this bit.

Bit 3 A read operation returns the result of the last write operation to this bit.

Bit 4 This bit toggles on each refresh request.

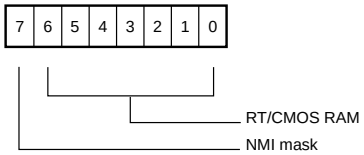
Bit 5 This bit reflects the condition of the timer 2 output latch.

Bit 6 This bit reflects the condition of the I/O check latch. If the bit is set to 1 an I/O check has occurred.

Bit 7 This bit reflects the condition of the Parity check latch. If the bit is set to 1 a Parity check has occurred.

RTC RAM/NMI mask

This port at I/O location 0070h controls the NMI mask and the index register for accessing the RT/CMOS RAM. The bit significance is given below.



Bits 0-6 These bits define the RT/CMOS RAM location to be accessed by the following read/write operation to 0071h.

Bit 7 With this bit set to 1 Non-maskable interrupts (NMI) are enabled. With this bit set to 0 NMI is disabled. A system reset sets this bit to 0.

The RT/CMOS RAM has a data port at I/O location 0071h. the following table lists the contents of the CMOS RAM.

Address	Function
Real time clock data	
00h	seconds
01h	alarm seconds
02h	minutes
03h	alarm minutes
04h	hours
05h	alarm hours
06h	day of week
07h	date
08h	month
09h	year
0Ah	status register A
0Bh	status register B
0Ch	status register C
0Dh	status register D
0Eh	Diagnostic status
0Fh	Shut-down status
Configuration data	
10h	diskette drive
11h	first hard disk drive
12h	second hard disk drive
13h	reserved
14h	equipment installed
15h	memory size in K (low byte)
16h	memory size in K (high byte)
17h	expanded memory size in K (low byte)
18h	expanded memory size in K (high byte)
19h-31h	reserved
32h-33h	configuration CRC
34h-36h	reserved
37h	date century
38h-3Eh	reserved
3Fh	checksum

SCAMP registers

This section identifies the ports used by, and the ports indexed in, the VL82C311. A full description of the ports is given in the manufacturers data sheet.

The SCAMP chipset uses a number of ports in the E8 to FFh range. The ports used are identified in the table below:

Port	Title
E8	EMS index register
E9	reserved
EA	EMS data port low byte
EB	EMS data port high byte
EC	Configuration index register
ED	Configuration data register
EE	Fast A20
EF	Fast reset
F0	Coprocessor busy clear
F1	Coprocessor reset
F4	Slow CPU
F5	Fast CPU
F8	Coprocessor
F9	Configuration disable
FA	Coprocessor
FB	Configuration enable
FC	Coprocessor
FE	Coprocessor

Note

Ports which are not specifically mentioned in the table are not used by the chipset.

EMS index register and data ports

The SCAMP chipset provides a LIM 4.0 compliant EMS system. The EMS index register is used to access 36 mapping registers through the two data ports. For further information on EMS refer to the LIM 4.0 specification.

The SCAMP EMS system is configured using the EMS configuration registers.

Configuration index and data registers

The configuration index register is used to access the SCAMP configuration registers through the configuration data port. To access a particular register write the index of the register to the configuration index register then access the register via the configuration data port.

Index (hex)	Register
0	Version
2	Slot pointer
3	DRAM map
5	DRAM control
6	Refresh control
7	Clock control
0A	Reserved
0B	EMS configuration 1
0C	EMS configuration 2
0E	A0000-BFFFFh segment access control
0F	C0000-CFFFFh segment access control
10	D0000-DFFFFh segment access control
11	E0000-FFFFFh segment access control
13	Reserved
14	Miscellaneous control
15	ROM and DMA control
16	Bus control

Apricot ports

A block of 16 ports between 0120h and 012Fh are reserved for Apricot specific functions.

Port	Function
120	LAN LED
121	1.6 Mbyte floppy
122	reserved
0123, 0124	Option ROM page
0125-0127	reserved
128	Token ring daughterboard
0129-012B	reserved
012C	microphone level control
012D-012F	reserved

LAN LED

Only bit 0 of this port is used.

When it is set low (default) the LAN LED is not lit. When it is set high the LAN LED is lit.

1.6 Mbyte floppy Only bit 0 of this port is used.

When it is set low (default) it indicates that a 2 Mbyte floppy drive is fitted. When it is set high it indicates that a 1.6 Mbyte floppy drive is fitted (Japanese market only).

Note

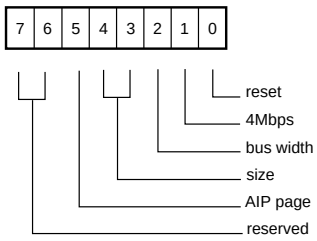
The function of this port is different on Rev C system boards. Refer to Appendix B for further information.

Option ROM page These two registers are used to select a 16K page within the 64K option ROM which has a base address of 0C0000h.

Only bit 0 is used in each of these ports. The following table shows the start address of the page selected for each combination of bit 0 of ports 0123h and 0124h.

0124h	0123h	Start address
0	0	0000h
0	1	4000h
1	0	8000h
1	1	C000h

Token-ring daughterboard



Bit 0 This bit is used to reset the Token-Ring daughterboard. The values written to bits 1 to 4 become active only after a reset. A reset casuses all data and register settings to be lost. The steps necessary to reset the daughterboard and change the settings controlled by bits 1 to 4 are:

write the required value to 0128h with bit 0 set to 0
write the required value to 0128h with bit 0 set to 1
wait at least 15µs
write the required value to 0128h with bit 0 set to 0

Bit 1 This bit selects between 4 and 16Mbps operation. When set to 0 16Mbps operation is selected, when set to 1 4Mbps is selected.

Bit 2 This bit selects between 8 and 16-bit modes. When set to 0 8-bit operation is selected, when set to 1 16-bit is selected.

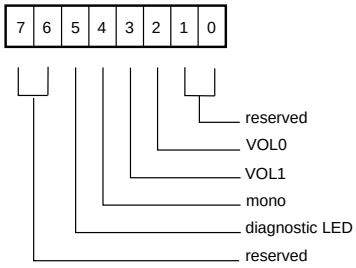
Bits 3, 4 These two bits select the size of page used to access the Token Ring daughterboard's shared RAM. The default window size is 16Kbytes.

4	3	Page size
0	0	16 Kbytes
0	1	8 Kbytes
1	0	64 Kbytes
1	1	32 Kbytes

Bit 5 This bit selects one of the two PROM pages. When set to 0 page 1 is selected, for an 8-bit adapter. When set to 1 page 2 is selected, for a 16-bit adapter. This bit should normally be set to the same value as the bus width bit (bit 2).

Bits 6, 7 Reserved.

Microphone level control



Bits 0, 1 Reserved.

Bits 2, 3 These two bits control the sensitivity of the microphone input.

Bit		Input level (rms)
3	2	
0	0	7.75mV
0	1	77.5mV
1	0	0.775V
1	1	2V

Bits 4 When this bit is low (default) the audio subsystem operates in stereo mode. When high the audio system operates in mono mode.

Bit 5 When this bit is low (default) the diagnostic LED on the system board is lit. When it is set high the LED is not lit.

Bits 6,7 Reserved.

Note

The function of this port is different on Rev C system boards. Refer to Appendix B for further information.

Hard disk drive controller registers

The hard disk drive embedded controller is accessed at the locations given in the following table.

Address	R/W	Function
01F0	R/W	Data register
01F1	R	Error register
01F1	W	Write precompensation cylinder register
01F2	R/W	Transfer sector count
01F3	R/W	Starting sector count
01F4	R/W	Low byte of cylinder number
01F5	R/W	High byte of cylinder number
01F6	R/W	Drive/head select register
01F7	R	Status register
01F7	W	Command register
03F6	R	Fixed disk status register
03F6	W	Fixed disk control register
03F7	W	Fixed/floppy disk digital input register

These ports are defined in ANSI specification: ATA (AT attachment) X3T9.2/9-143.

Serial port controller registers

Each serial port controller has several accessible registers which are for control and data transfer. The following table shows where each register is located in I/O space for each port.

COM1	COM2	R/W	Register
03F8	02F8	W	Transmit data register (DLAB=0)
03F8	02F8	R	Receive data register (DLAB=0)
03F8	02F8	R/W	Divisor latch, low byte (DLAB=1)
03F9	02F9	R/W	Divisor latch, high byte (DLAB=1)
03F9	02F9	R/W	Interrupt enable register (DLAB=0)
03FA	02FA	R	Interrupt ID register
03FB	02FB	R/W	Line control register
03FC	02FC	R/W	Modem control register
03FD	02FD	R	Line status register
03FE	02FE	R	Modem status register
03FF	02FF	R/W	Scratch register

The registers are described in detail in the manufacturers data sheets.

Note

Rev C system boards are not fitted with the second serial port (COM2).

Ethernet controller

The Ethernet controller on the LS Pro system board uses a block of 17 I/O ports from 0300h to 0310h.

Port	Function
300	82596 PORT address
0301-0303	reserved
304	82596 CA address
0305-0307	reserved
0308-030F	Ethernet ID PROM
310	Ethernet status register

82596 PORT address This is a 16-bit write only port. The data definition of this port is given in the manufacturers data book.

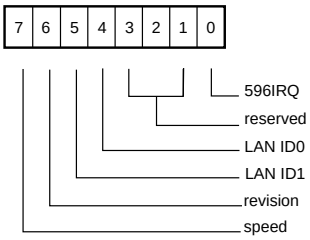
82596 CA address This is a 16-bit write only port that has no data associated with it. An access to this port activates the CA control signal. A definition of the operation of this port is given in the manufacturers data book.

Ethernet ID PROM The lower six bytes of the ID PROM contain the six byte Ethernet ID.

Port	ID byte
308	0
309	1
030A	2
030B	3
030C	4
030D	5

030Eh is reserved, and 030Fh contains a checksum for the other seven bytes.

Ethernet status register This port has different functions in read and write cycles.



Bit 0 This bit returns the current state of the IRQ line from the 82596 Ethernet coprocessor.

Bits 1-3 Reserved.

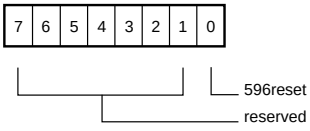
Bits 4, 5 These two bits indicate the presence or absence of a Token-Ring daughterboard as shown in the following table

5	4	Significance
0	0	Token-ring fitted
0	1	reserved
1	0	reserved
1	1	No Token-Ring

Bit 6 This bit indicates the revision level of the system board. Revision C boards return a 0, revision D boards return a 1.

Bit 7 This bit indicates the speed of the processor fitted to the system board. Returns a 1 when a 33MHz processor is fitted. A 0 indicates a 25MHz processor.

Write cycles



Bit 0 This bit is used to reset the 82596 Ethernet coprocessor. To reset the 82596 the following sequence must be followed:

write a 0 to bit 0 of 310h
write to port 08Eh
write a 1 to bit 0 of 310h
write to port 08Eh
write a 0 to bit 0 of 310h
write to port 08Eh

Bits 1-7 Reserved.

Business audio

The Apricot business audio subsystem occupies a block of 8 ports from 0388h to 038Fh.

Port	Function
0388-038B	reserved
038C	Address
038D	channel 0 data
038E	reserved
038F	channel 1 data

The following descriptions are brief outlines of the function of the ports. A full description is given in the manufacturers data sheet.

Address *Write*

When written to the address port acts as an index to the data ports for channels 0 and 1. The value written to 038Ch is a pointer to a location accessed at 038Dh or 038Fh.

Read

When read the address port returns status information.

Data ports Each channel has a data port associated with it. The ports provide access to a group of locations. The address port is used to index these locations.

Floppy disk controller

The floppy disk controller has a variety of registers which return status information and provide control over its operation.

Port (Hex)	R/W	Function
03F2	R/W	Digital output register
03F4	R	Main status register
03F5	R/W	Data register
03F7	R	Fixed/floppy digital input register
03F7	W	Data rate select

A full description of the operation of the floppy controller is given in the manufacturers data sheet.

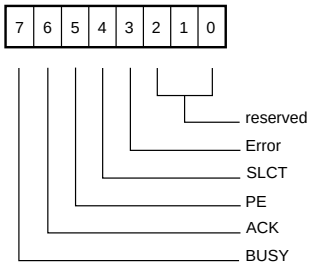
Parallel port controller

The registers described below are the parallel port control, data and status ports.

Data Address	Status Address	Control address
03BC	03BD	03BE

Data address port The Data Address port is an 8-bit data port. A write operation to this port immediately presents data to connector pins; a read operation produces the data that was last written to it.

Status Port The Status Port is a read-only port. A read operation to this port presents the system micro-processor with the interrupt pending status of the connector pins as shown below. An interrupt is pending when the interrupt status bit is set to 0.



Bits 0-2 Reserved

Bit 3 This bit represents the current state of the printer ERROR Signal. When this bit is set to 0 the printer has encountered an error condition.

Bit 4 This bit represents the current state of the select (SLCT) signal. When this bit is set to 1 the printer has been selected.

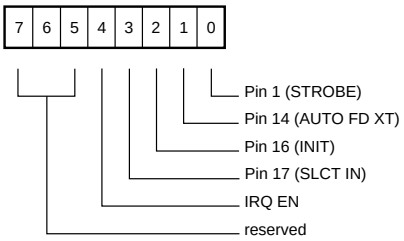
Bit 5 This bit represents the state of the printer paper end (PE) signal. When this bit is set to 1 the printer has detected the end of the paper.

Bit 6 This bit represents the current state of the printer acknowledge ACK signal. When this bit is set to 0 the printer has received a character and is ready to accept another.

Bit 7 This bit represents the state of the BUSY signal. When the signal is active the printer is busy and cannot accept data.

Parallel control port

This parallel control port is a read or write port. A write operation to this port latches the six least significant data bits of the bus. The sixth bit corresponds to the direction control bit and is only applicable in extended mode. The significance of the bits is shown below. A read operation to this port presents the system microprocessor with the data that was last written to the port, with the exception of the write-only direction bit.



Bit 0 This bit controls the strobe signal to the printer. When this bit is set to 1 data is pulse-clocked into the printer

Bit 1 This bit controls the automatic feed XT (AUTO FEED XT) signal. When this bit is set to 1, the printer will automatically line feed after each line is printed.

Bit 2 This bit controls the initialize printer (INIT) signal. When this bit is set to 0, the printer is selected.

Bit 3 This bit controls the select in (SLCT IN) signal. When this bit is set to 1, the printer is selected.

Bit 4 This bit enables the parallel port interrupt. When this bit is set to 1 an interrupt occurs when the acknowledge signal changes from active to inactive.

Bits 5-7 Reserved

Video DAC

The video digital to analogue converter (DAC) is enabled in the video controller and contains a colour lookup table and three DACs. Four I/O ports are used to access the Video DAC.

Port	Read/Write	Function
03C6	R/W	Pixel Mask
03C7	R	DAC state register
03C7	W	Pixel address (read mode)
03C8	R/W	Pixel address (write mode)
03C9	R/W	Pixel data register

These registers comply with the VGA standard. They are described in detail in the manufacturers data sheet.

VGA registers

The registers which configure and control the VGA are divided into six groups. Each group of registers is accessed by a number of I/O port addresses. The register groups and port addresses are shown in the list below.

Registers	Attributes	Address
General Registers		
Miscellaneous output register	WMC	03C2h
	RMC	03CCh
Input status register 0	RMC	03C2h
Input status register 1	RM	03BAh
	RC	03DAh
Feature control register	WM	03BAh
	WC	03DAh
	RMC	03CAh
Video subsystem enable register	RW	46E8h
Sequencer registers		
Sequencer index registers	RWMC	03C4h
Sequencer data registers	RWMC	03C5h
CRT controller registers		
Index register	RWM	03B4h
	RWC	03D4h
CRT controller data register	RWM	03B5h
	RWC	03D5h
Graphics controller registers		
Index register	RWMC	03CEh
Other graphic registers	RWMC	03CFh
Attribute controller registers		
Index register	RWMC	03C0h
Attribute controller data registers	WMC	03C0h
	RMC	03C1h

DAC registers

The DAC registers are described on page 5/18.

R - read
W - write
M - monochrome
C - colour

All the above registers are functionally identical to the IBM standard VGA equivalents.

The groups of registers are described in the following sections. There are several pairs of registers an index register and a data register. In these cases the index register is a pointer to a number of other registers which are accessed via the accompanying data register.

General registers

The general registers cover a number of miscellaneous hardware functions. They are used to select the I/O address range, to enable RAM, select dot clock speed, set sync. signal polarity and write to bits on the feature connector. In the read mode, they give access to two status registers.

The registers use two port addresses and are listed below:

Register	Address
Miscellaneous output register	03C2h (WMC)
	03CCh (RMC)
Input status register 0	03C2h (RMC)
Input status register 1	03BAh (RM)
	03DAh (RC)
Feature control register	03BAh (WM)
	03DAh (WC)
	03CAh (RWMC)

R - read
W - Write
M - monochrome
C - colour

These registers are standard VGA registers and are not described in further detail here.

Sequencer registers

The sequencer register controls memory plane selection and shift register timing functions. The registers are accessed by using index and data registers. To access a register, first write to the index register with the index of the register to be accessed as the data then write to the data register with the data to be loaded.

Register	Address
Sequencer index register	03C4h (RWMC)
Sequencer data register	03C5h (RWMC)

R - read
W - write
M - monochrome
C - colour

The following table shows the index and the registers that are accessed via the index.

Register	Index
Reset	00h
Clocking mode	01h
Map mask	02h
Character map select	03h
Memory mode	04h

These are standard VGA registers and are not described in further detail here.

CRT Controller registers

The CRT controller registers handle the data associated with the CRT. The registers are accessed by using index and data registers. To access a register, first write to the index register with the index of the data register to be accessed, then read or write to the data register.

Register	**Address**
CRT controller index register	03B4h (RWM)
	03D4h (RWC)
CRT controller data register	03B5h (RWM)
	03D5h (RWC)

R - read
W - write
M - monochrome
C - colour

The following table shows the index and the registers which can be accessed via the index.

Register	**Index**
Horizontal total	00h
Horizontal display enable end	01h
Start horizontal blanking	02h
End horizontal blanking	03h
Start horizontal retrace pulse	04h
End horizontal retrace	05h
Vertical total	06h
Overflow	07h
Preset row scan	08h
Maximum scan line	09h
Cursor start	0Ah
Cursor end	0Bh
Start address high	0Ch
Start address low	0Dh
Cursor location high	0Eh
Cursor location low	0Fh
Vertical retrace start	10h
Vertical retrace end	11h
Vertical display enable end	12h
Offset	13h
Underline location	14h
Start vertical blank	15h
End vertical blank	16h
CRTC mode control	17h
Line compare	18h

These are standard VGA registers and are not described in further detail here.

Graphics controller registers

The graphics controller registers handle the reading, writing and other manipulations of the graphics data.

The registers are accessed by using index and data registers. To access a register, first write to the index register with the index of the register to be accessed, then write to the data register with the data to be loaded.

Register	Address
Graphics controller index register	03CEh (RWMC)
Graphics controller data register	03CFh (RWMC)

R - read
W - write
M - monochrome
C - colour

The following table shows the index and the registers which can be accessed via the index.

Register	Index
Set/reset	00h
Enable set/reset	01h
Colour compare	02h
Data rotate	03h
Read map select	04h
Graphics mode	05h
Miscellaneous	06h
Colour don't care	07h
Bit mask	08h

These are standard VGA registers and are not described in further detail here.

Attribute controller registers

These registers control the screen attributes. In text mode, these are the colour, intensity and blinking of the characters, and the background. In graphics mode, you can select the colour to each pixel.

The four memory planes generate a four bit colour code for each pixel. The colour plane enable register allows each memory plane to be enabled or disabled.

Each colour code is translated by a palette register into video signals to drive the monitor.

The attribute controller registers are addressed by a single I/O port address.

The index register is an index to the attribute data registers. Unlike the other index registers of the VGA adapter, the attribute index and data registers are located at the same I/O address. Alternate writes are to the index and then the data register.

Register	Address
Attribute controller index register	03C0h (RWMC)
Attribute controller data register	03C0h (WMC)
	03C1h (RMC)

R - read
W - write
M - monochrome
C - colour

The following table shows the index values and the registers that are accessed by them:

Register	Index
Palette	00h to 0Fh
Attribute mode control	10h
Overscan control	11h
Colour plane enable	12h
Horizontal pixel panning	13h
Colour select	14h

These are standard VGA registers and are not described in further detail here.

CL-GD542X Extension registers

The CL-GD542X video controllers have a number of extension registers. These registers are accessed via the index and data registers of the standard VGA CRT Controller, Sequencer and Graphics Controller registers.

The extension registers are listed in tables which follow. A full description of the registers is included in the manufacturers data sheet and is not reproduced here.

The table below lists the CRT Controller register extensions accessed at 03B4h and 03B5h or 03D4h and 03D5h.

Register	**Index**
Interlace end	19
Interlace control	1A
Extended display controls	1B
Part status	25
ID register	27

The table below lists the Sequencer register extensions accessed at 03C4h and 03C5h.

Register	**Index**
Unlock all extensions	6
Extended sequencer mode	7
EEPROM control	8
Scratch pad 0	9
Scratch pad 1	A
VCLK numerators 0-3	B-E
DRAM control	F
Graphics cursor Y position	10
Graphics cursor X position	11
Graphics cursor attributes	12
Graphics cursor pattern address offset	13
Scratch pad 2 *	14
Scratch pad 3 *	15
Performance tuning *	16
Signature generator control	18
Signature generator result (low byte)	19
Signature generator result (high byte)	1A
VCLK0-3 denominator and post-scalar value	1B-1E
BIOS ROM write enable and MCLK select	1F

* indicates that the register is present in the CL-GD5426, but not the CL-GD5422.

The table below lists the Graphics Controller register extensions accessed at 03CEh and 03CFh.

Register	Index
Offset register 0	9
Offset register 1	A
Graphics controller mode extensions	B
Colour key *	C
Colour key mask *	D
16-bit pixel BG colour (high byte)	10
16-bit pixel FG colour (high byte)	11
BLT width low *	20
BLT width high *	21
BLT height low *	22
BLT height high *	23
BLT destination pitch low *	24
BLT destination pitch high *	25
BLT source pitch low *	26
BLT source pitch high *	27
BLT destination start low *	28
BLT destination start mid *	29
BLT destination start high *	2A
BLT source start low *	2C
BLT source start mid *	2D
BLT source start high *	2E
BLT mode *	30
BLT start/status *	31
BLT raster operation *	32
Transparent colour select low *	34
Transparent colour select high *	35
Source transparent colour mask low *	38
Source transparent colour mask high *	39

* indicates that the register is present in the CL-GD5426, but not the CL-GD5422.

In addition to the registers listed above the CL-GD542X extends the functionality of several of the standard VGA registers. While operating in standard VGA modes these extensions are inactive, and the registers comply with the VGA standard.

Note

Revision C of the LS Pro system board is equipped with a CL-GD5410 video controller. This uses a different set of extension registers. Refer to Appendix B for further information.

A SPECIFICATIONS

System unit

Width	322mm
Height	53mm
Depth	343mm
Weight	3.9kg (approx)

Keyboard

Width	485mm
Depth	204 mm
Weight	1.4 kg

Apricot SVGA colour monitor

Width	351 mm
Height	327 mm
Depth	384 mm
Weight	11.5 kg
Resolution	800x600 non-interlaced (maximum)
	1024x768 interlaced (maximum)

CRT

Size	14"
Pitch	0.28 mm

HiVision 14" Low Emission multi sync

	Width	351 mm
	Height	354 mm
	Depth	400 mm
	Weight	14.5 kg
	Resolution	1024x768 maximum
CRT	Size	14"
	Viewable	13"
	Pitch	0.26mm

HiVision 17" Low Emission multi sync

	Width	405 mm
	Height	370 mm
	Depth	480 mm
	Weight	25.9 kg
	Resolution	1024x768 max
CRT	Size	17"
	Viewable	16"
	Pitch	0.26mm

Specifications

Environmental (operational)

Temperature ..... 5 to 35 °C
Humidity ..... 10% to 80% relative humidity with no condensation

Power supply

AC input

110-120V ..... 3.0A(max)
220-240V ..... 2.5A(max)
50-60Hz

Note

The AC input ratings include 1.5A for the AC output.

AC output

110-120V ..... 1.5A(max)
220-240V ..... 1.5A(max)

DC output *40 Watts (total)*

Voltage	Current	Tolerance (pk to pk)	Ripple
+5V	5 Amps	±0.1V	150mV
+12V	1 Amp	±0.4V	100mV
-12V (nominal)			
-12.1V (actual)	200mA	±0.6V	150mV

Note

The +12V output has a rated surge capacity of 2A for 10 seconds.

MTBF > 50000 hours

Input to output isolation ..... withstand minimum of 3750V RMS for 1 minute
Input to output resistance ..... minimum of 100Mohms @ 500V input
Input to earth isolation ..... withstand minimum of 1275V RMS for 1 minute
Earth continuity ..... maximum 0.1ohm at 20A current flow

Sony MP-F17W

Height ..... 25.4 mm
Width ..... 101.6 mm
Depth ..... 150.0 mm
Weight ..... 425 g

Rotational speed ..... 300 rpm
Track density ..... 135 TPI
Cylinders 80
Tracks 160
R/W heads 2
Encoding Method ..... MFM

Capacity

Unformatted ..... 2Mbytes (HD disks)
Formatted ..... 1.44 Mbytes (HD disks)
Recording Density ..... 17434 BPI
Burst transfer rate ..... 500 Kbits/second

Power Consumption

+5V ..... 220 mA (read/write mode)

Access Times

Track to track ..... 3 mS
Settling Time ..... 15 mS

Quantum ELS drives

Height 25.4mm
Depth 146.2mm
Width 101.6mm
Weight ..... 0.41 Kg

Environmental

Ambient temperature

Operating ..... 0 to 50 °C
Non-operating ..... -40 to 65 °C

Humidity

Operating ..... 8 to 85% RH, noncondensing
Non-operating ..... 5 to 95% RH, noncondensing

Shock

Operating ..... 10G with 11ms pulse width, half sine
Non-operating ..... 70G with 11ms pulse width, half sine
MTBF ..... 250,000 power on hours

Power

+5V ± 5% ripple<50mV

Current ..... 0.23A typical

+12V ± 10% ripple<100mV

Current ..... 0.17A (typical) 0.76A (max)

Error rates

Recovered data error rate ..... < 1 per 10^{10} bits read
Unrecoverable error rate ..... < 1 per 10^{14} bits read
Seek error rate ..... < 1 per 10^{6} seeks

Physical

Rotation speed 3663rpm
Recording density ..... 38,600 bpi
Track density ..... 1800 tpi
Cylinders 1528
Disks 1/2
Tracks 3056/4584/6112
Heads 2/3/4
Capacity (formatted) ..... 85/127/170 Mbytes

Specifications

Seek time (ms)

Average	18
Track to track	5.5
Full stroke	34

Maximum data transfer rates	Buffer to AT-bus	4.0 Mbytes/second
	Disk to Buffer	3.0 Mbytes/second

Maxtor 7213A

Height	25.4mm
Depth	146.1mm
Width	101.6mm
Weight	0.5 Kg

Environmental — *Ambient temperature*

Operating	5 to 50 °C
Non-operating	-40 to 65 °C

Humidity

Operating	8 to 80% RH, noncondensing
Non-operating	8 to 80% RH, noncondensing

Shock

Operating	10G with 11ms pulse width, half sine
Non-operating	70G with 11ms pulse width, half sine
MTBF	150,000 power on hours

Power	+5V ± 5% ripple<100mV Current	0.3A typical
	+12V ± 8% ripple<100mV Current	0.25A (typical) 0.70A (max)
Error rates	Hard read errors	< 1 per 10^{13} bits read

Physical	Rotation speed	3551rpm
	Recording density	42700 bpi
	Track density	1973 tpi
	Cylinders	1698
	Disks	2
	Heads	4
	Capacity (formatted)	200Mbytes

Quantum LPS 240AT

Height	25.4mm
Depth	146.2mm
Width	101.6mm
Weight	0.48 Kg

Environmental

Ambient temperature

Operating	5 to 55 °C
Non-operating	-40 to 70 °C

Humidity
Operating ..... 8 to 85% RH, noncondensing
Non-operating ..... 5 to 95% RH, noncondensing

Shock
Operating ..... 6G with 11ms pulse width, half sine
Non-operating ..... 70G with 11ms pulse width, half sine

MFBT ..... 250,000 power on hours

Power consumption

Idle ..... <3.9 Watts
40% seek ..... <4.9 Watts

Error rates

Unrecoverable error rate ..... < 1 per 10^{14} bits read
Seek error rate ..... < 1 per 10^{6} seeks

Physical

Rotation speed 4306rpm
Recording density ..... 38,000 bpi
Track density ..... 1900 tpi
Disks 2
Tracks (per surface) 1800
Heads 4

Capacity (formatted) ..... 245 Mbytes

Seek time (ms)
Average 16
Track to track 4
Full stroke 30

Maximum data transfer rates

Buffer to AT-bus ..... 5.0 Mbytes/second
Disk to Buffer ..... 3.8 Mbytes/second

Seek time (ms)
Average 17
Track to track 4
Full stroke 30

Quantum LPS525AL

Height 25.4mm
Depth 146mm
Width 101.6mm
Weight ..... 0.5 Kg

Specifications

Environmental	*Ambient temperature*	
	Operating	0 to 55 °C
	Non-operating	-40 to 65 °C
	Humidity	
	Operating	8 to 80% RH, noncondensing
	Non-operating	5 to 95% RH, noncondensing
	Shock	
	Operating	10G with 11ms pulse width, half sine
	Non-operating	60G with 11ms pulse width, half sine
	MFBT	250,000 power on hours
Power	*+5V*	
	Current	0.64A (average) 0.72A (maximum)
	Power	3.2W average
	+12V	
	Current	0.70A (average) 2.0A (maximum)
	Power	8.4W average
Error rates	Unrecoverable error rate	< 1 per 10^{12} bits read
	Seek error rate	< 1 per 10^{14} seeks
Physical	Rotation speed	4500rpm
	Recording density	36,700 fci
	Track density	2,670 tpi
	Cylinders	2234
	Disks	3
	Tracks	14,688
	Heads	6
	Capacity (unformatted)	525 MB
	Seek time (ms)	
	Average	10
	Track to track	3
	Full stroke	18
Maximum data transfer rates	To AT-bus	5.0 Mbytes/second

This manual describes the LS Pro fitted with a Revision D system board. During the first eight months of production the LS Pro range was fitted with Revision C system boards. This Appendix helps you identify which revision of system board you have, and describes the differences between revisions C and D.

Identifying system board revisions

External identification

The only way to identify which revision of system board is fitted in the system unit without obtaining access to the system board is to refer to the model number label on the rear of the system unit.

Systems fitted with a Revision C system board have model numbers starting BN.

Systems fitted with a Revision D system board have model numbers starting BO.

Internal identification

The easiest way to identify which revision of system board is fitted in the system unit when you have obtained access to the system board is to refer to the identification label at the front left of the system board.

Both revisions of board are labelled PC223. Revision C boards are labelled PC223/C, PC223/C1 or PC223/C2. Revision D boards are labelled PC223/D2.

Differences

There were two major changes between revision C and revision D.

1. Video controller

   Where the revision D board is fitted with either a CL-GD5422 or CL-GD5426 video controller the revision C board uses a CL-GD5410. Since the 5410 video BIOS is more compact than the 542X BIOS of the Rev D board the memory map between C0000h and 100000h (768k and 1M) is different on Rev C boards. Details on the CL-GD5410 and the Rev C memory map are given later in this appendix.

2. Serial port

   Revision D of the system board is fitted with an 16C452 serial and parallel port controller which provides one parallel and two serial ports. Revision C of the system board is fitted with an 16C451 serial and parallel port controller which provides one parallel and one serial port (COM1).

CL-GD5410

The video adapter on revision C of the LS Pro system board is based on a Cirrus Logic CL-GD5410 chip. The CL-GD5410 contains all the elements of a VGA controller, except display memory, providing 100% compatibility with the IBM VGA standard.

The video adapter consists of the GD5410 video controller, 1 Mbyte of display memory, a frequency synthesizer and a 7.6mA current reference.

The frequency synthesizer is controlled by the GD5410 and is used to generate the video clocks for all video modes. Video dot clocks vary from 25 to 65 MHz depending on video mode.

Software support is provided by a video BIOS included in the system BIOS.

In addition to full compatibility with the VGA standard the GD5410 supports a range of enhanced video modes. Seven enhanced modes are supported in the BIOS.

The video modes available are given in the following table:

Mode	Type	Colours	Displayed Chars	Character Cell	Pixels	Note
0, 1	Text	16/256K	40x25	9x16	360x400	
2, 3	Text	16/256K	80x25	9x16	720x400	
4, 5	Graphics	4/256K	40x25	8x8	320x200	
6	Graphics	2/256K	80x25	8x8	640x200	
7	Text	-	80x25	9x16	720x400	
D	Graphics	16/256K	40x25	8x8	320x200	
E	Graphics	16/256K	80x25	8x8	640x200	
F	Graphics	-	80x25	8x14	640x350	
10	Graphics	16/256K	80x25	8x14	640x350	
11	Graphics	2/256K	80x30	8x16	640x480	
12	Graphics	16/256K	80x30	8x16	640x480	
13	Graphics	256/256K	40x25	8x8	320x200	
2E	Graphics	256/256K	80x30	8x16	640x480	1
30	Graphics	256/256K	100x37	8x16	800x600	1
37	Graphics	16/256K	128x48	8x16	1024x768	1
38	Graphics	256/256K	128x48	8x16	1024x768	1
64, 6A	Graphics	16/256K	100x37	8x16	800x600	1
7A	Graphics	64K/64K	80x30	8x16	640x480	1
7B	Graphics	64K/64K	100x37	8x16	800x600	1

Notes

1. *These are enhanced video modes.*

Sync signals output to the monitor are at TTL levels while the analogue video outputs are at 0 to 0.7 volts.

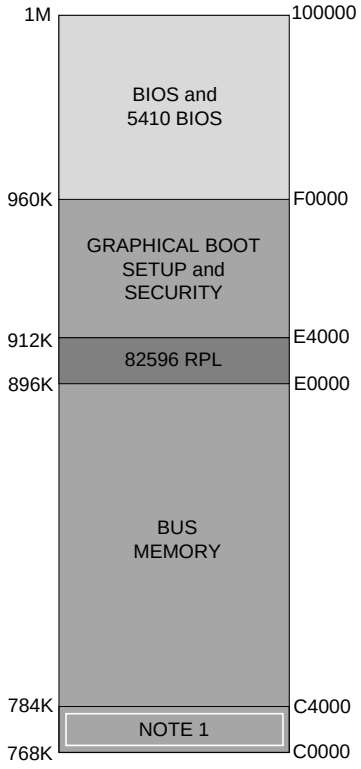
Extension registers

The CL-GD5410 video controller has a number of Extension registers. By default these registers are accessed using the Graphics Controller index and data registers.

The extension registers are listed in tables which follow. A full description of the registers is included in the manufacturers data sheet and is not reproduced here.

Design revision	AA
Reserved	AC-AD
Alternate extension decode high	AE
Alternate extension decode low	AF
Reserved	B0-B9
Scratch register 5-0	BA-BF
Attribute and graphics control	C0
Cursor attributes	C1
Graphics controller memory latches 0-3	C2-C5
Reserved	C6-C7
RAMDAC controls	C8
Graphics and attribute test	C9
Reserved	CA-DF

Memory map



1. *This area is occupied by the ROM in the option ROM socket if it is fitted.*

The 5410 BIOS is integrated with the system BIOS in the F0000h to FFFFFh region. All the code in the region E0000h to EFFFFh region is used only at boot. Thus with the option ROM socket empty the region from C0000h to EFFFFh is available as DOS UMB space.

Revision C system board

I/O registers

The function of two of the Apricot specific I/O ports are different on the revision C system board. The two ports are 121h and 12Ch.

On revision C of the system board, port 121h is used to control the diagnostic LED on the system board. When bit 0 of this port is low (default) the diagnostic LED is lit. when it is set high the diagnostic LED is extinguished.

Bits 4 and 5 of port 12Ch are reserved on revision C system boards. 12Ch is used only to control the microphone level.

System memory

Revision C systems may have 2 or 4 Mbytes of RAM soldered to the system board and provide an additional option ROM socket.

When 4 Mbytes of RAM is installed during manufacture four SIMM sockets are fitted. When 2 Mbytes of RAM is installed six SIMM sockets are fitted.

SIMMs must be installed in pairs, upgrades of 2 and 8 Mbytes are available. The 2 Mbyte upgrade contains two 60nS 1Mx9 SIMMs, the 8 Mbyte upgrade contains two 60nS 4Mx9 SIMMs.

The following table identifies the valid upgrade combinations.

System board capacity (Mbytes)	Upgrade to (Mbytes)	Bank			Note
		1	2	3	
2	4	2	-	-	
2	6	2	2	-	
2	8	2	2	2	1
2	12	2	8	-	
2	16	-	8	8	2
4	6	N/A	2	-	
4	8	N/A	2	2	1
4	12	N/A	8	-	
4	16	N/A	8	8	2

Notes

1. *For both system board RAM capacities an alternative method of achieving 8 Mbytes of RAM is to install an 8 Mbyte upgrade in bank 2 and leave the other bank (or banks) empty. This configuration disables the RAM soldered to the system board.*

2. *When banks 2 and 3 are both occupied by 8 Mbyte upgrades the RAM soldered to the system board is disabled.*

Each time that the computer is powered-up, the power on self test (POST) is executed. The POST tests:

- processor system
- memory
- hard disk drive
- floppy disk drive and controller
- keyboard
- ROM checksum
- system configuration
- video system
- real time clock
- system timer
- correct boot disk

If all the tests are completed sucessfully, one short beep will be heard from the loudspeaker in the system unit.

If a failure is encountered, one or more of the following responses will be obtained:

- a blank screen
- no beep or more than one beep
- an error message

If a blank screen is obtained, check that power is applied to both the system unit and monitor.

Check that all cables are properly connected and that the system is properly configured.

Error beep codes

If more than one beep code is heard, make a note of the sequence of beeps and refer to the following table to determine the cause of the error. As an example, the beep sequence '1-3-3' represents: a single beep followed by a group of three beeps, followed by another group of three beeps.

Beep sequence	Error
1-1-3	CMOS RAM read/write test failure
1-1-4	BIOS ROM checksum failure
1-2-1	Programmable interval timer failure
1-2-2	DMA initialisation failure
1-2-3	DMA page register read/write test failure
1-3-1	RAM refresh verification failure
1-3-3	1st 64k RAM data line failure (multibit)
1-3-4	1st 64k RAM data odd/even logic failure
1-4-1	1st 64k RAM address line failure
1-4-2	1st 64k RAM parity failure
1-4-3	Fail-safe timer test in progress
1-4-4	Software NMI port test in progress
2-1-1	1st 64k RAM data line failure (bit 0)
2-1-2	1st 64k RAM data line failure (bit 1)
2-1-3	1st 64k RAM data line failure (bit 2)
2-1-4	1st 64k RAM data line failure (bit 3)
2-2-1	1st 64k RAM data line failure (bit 4)
2-2-2	1st 64k RAM data line failure (bit 5)
2-2-3	1st 64k RAM data line failure (bit 6)
2-2-4	1st 64k RAM data line failure (bit 7)
2-3-1	1st 64k RAM data line failure (bit 8)
2-3-2	1st 64k RAM data line failure (bit 9)
2-3-3	1st 64k RAM data line failure (bit A)
2-3-4	1st 64k RAM data line failure (bit B)
2-4-1	1st 64k RAM data line failure (bit C)
2-4-2	1st 64k RAM data line failure (bit D)
2-4-3	1st 64k RAM data line failure (bit E)
2-4-4	1st 64k RAM data line failure (bit F)
3-1-1	Slave DMA register failure
3-1-2	Master DMA register failure
3-1-3	Master interrupt mask register failure
3-1-4	Slave interrupt mask register failure
3-2-4	Keyboard controller failure
3-3-4	Screen memory failure
3-4-1	Screen initialisation failure
3-4-2	Screen retrace test failure

In addition to the error beep codes above the video BIOS on the revision D system board can return the following two error codes:

1-2	Old video adapter failed
1-3	Checksum failure/DAC failure/RAM error

Error messages which appear on the screen are in text form, not error codes. The appropriate action can then be taken. For example:

Error message

Not a boot diskette - strike F1 to retry boot

Action

Insert correct disk and reboot

INDEX

A

B

C

D

E

F

G

H

I

J

K

L

M

N

O

P

Q

R

S

T

U

V

W

Y

apricot

APRICOT COMPUTERS LIMITED
3500 PARKSIDE
BIRMINGHAM BUSINESS PARK
BIRMINGHAM B37 7YS

MITSUBISHI ELECTRIC

Part No 15050131
Revision No 01